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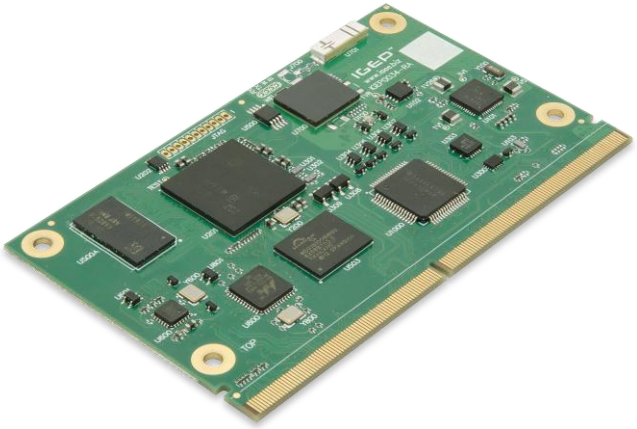

IGEP™ SMARC AM335x

HARDWARE REFERENCE MANUAL

SMARC module

SGeT STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

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1.1	01/20/2017	• First Review
2.0	11/12/2019	• Second Release (IGEP 0034-RBxx)

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1 USER INFORMATION

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2 INTRODUCTION

2.1 PRODUCT DESCRIPTION

The IGEP™ SMARC AM335x is an industrial ultra-low computer module based on AM335x processor family by Texas Instruments, featuring single ARM Cortex-A8 (with a speed up to 1 GHz).

It is an industrial computer module (it can work in a temperature range from -40ºC to +85ºC), in a very low profile according the standard form factor SMARC by SGET (its size is only 82,00 mm x 50,00 mm). With different combinations of RAM and Flash memory (see customized possibilities at chapter 2.4) and a complete list of interfaces and peripherals including 3D graphic accelerator, it can be the base for a complex industrial equipment or any other kind of application.

For development purposes there is also available an expansion board (IGEP™ SMARC EXPANSION) to complete the module. It can be used as the fastest way to develop the user's final application before the prototyping phase. This expansion board can be used with all IGEP™ SMARC modules.

Highlights:

- Fully tested, highly reliable, scalable, efficient and high performing board that allows customers to focus on their end application.
- Designed for industrial range purposes (temperature range: -40ºC to +85ºC).
- Form factor according to small size SMARC (82,00 mm x 50,00 mm).
- Easy connectivity through MXM3 graphic cards type connector: 314-pin, 0,5 pitch right angle.
- 1V8 I/O level digital signals.
- JTAG interface available.
- Based on Texas Instruments AM335x processor family, with ARM Cortex-A8.
- Two available Mbps Ethernet MAC+PHY interface: Fast (10/100 Mbps) and GBE (10/100/1000 Mbps)
- Flexible Flash Memory combinations (customized option).
- WiFi 802.11 b/g/n / Bluetooth 4.2 connectivity
- RAM memory size: Up to 512 MB.
- Flash memory size: Up to 512 MB.
- Low Power solution.
- Compatible with SMARC modules.

2.2 IGEP™ SMARC AM335x BENEFITS AND APPLICATIONS

There are a lot of advantages that developers will find in the IGEP™ SMARC AM335x series. Reducing the implementation time and saving costs on their designs. Amongst others, the main benefits are the following:

- Easy scalability between different modules (even with other processors) thanks to the SMARC standard.
- Compact and powerful core for new products.
- Robust and easy to mount due to the MXM3 314-pin connector.
- Reduced time to market.
- Low power consumption: Typical 1.5W.
- Industrial Temperature Range -40 to +85ºC.
- Extended life range product.

At the same time, it can be implemented in all kind of end applications. The followings are just a few ones, but the list can be as long as the imagination of the developers.

- Connected vending machines.
- Home / Building automation (IoT applications).
- Human Interface.
- Industrial Control.
- Test and Measurement.
- Artificial Intelligence

2.3 SMARC STANDARD

The IGEP™ SMARC AM335x accomplish the SMARC 2.0 version, which is defined by SGET.

The SMARC (“Smart Mobility Architecture”) is a computer Module definition targeting applications that require low power, low costs, and high performance. This standard is based on the former ULP-COM standard (Ultra Low Power Computer-on-Modules). The Modules will typically use ARM SoCs (System on Chip) families or similar.

SMARC standard defines two module sizes (82mm x 50mm and 82mm x 80mm). **All the available IGEP modules sizes 82mm x 50mm**. The Module PCBs have 314 edge fingers that mate with a low profile 314 pin (156 on TOP side and 158 on BOTTOM side) right angle connector. The module pins are designated as P1-P156 on the TOP side and S1 – S158 on the BOTTOM side. The connector is sometimes identified as a 321-pin connector, but 7 pins are lost to the key (4 on the TOP side and 3 on the BOTTOM side).

The Modules are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE and a single channel LVDS display transmitter are concentrated on the Module. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

2.4 SMARC FORM FACTOR FEATURE SUMMARY

Small form factor, low profile and low power edge-finger card format Module with pin-out optimized for ARM and x86 architecture processors; may also be used with low power, tablet oriented X86 and RISC devices.

- Two Module sizes:
  - 82mm x 50mm
  - 82mm x 80mm
- Carrier Board connector: 314 pin 0.5mm pitch R/A memory socket style connector
  - Originally defined for use with MXM3 graphics cards.
  - SMARC Module pin-out is separate from and not related to MXM3 pin-out.
  - Multiple sources for Carrier Board connector
  - Low cost
  - Low profile:
    - As low as 1.5mm (Carrier Board top to Module bottom)
    - Other stack height options available, including 2.7mm, 5mm, 8mm
    - Overall assembly height (Carrier Board top to tallest Module component) is less than 6mm
  - Excellent signal integrity – suitable for 2.5 GHz / 5 GHz / 8 GHz data rate signals such as PCIe Gen 1, Gen 2 and Gen 3.
  - Robust, vibration resistant connector.
- Module input voltage range: 3.0V to 5.25V
  - Allows operation from 3.6V nominal Lithium-ion battery packs.
  - Allows operation from 3.3V fixed DC supply.
  - Allows operation from 5.0V fixed DC supply.
  - Single supply (no separate standby voltage).
  - Module power pins allow 5A max.
- Low power designs
  - Fanless
  - Passive cooling
  - Low standby power
  - Design for battery operation
  - 1.8V default I/O voltage

2.5 IGEP™ SMARC AM335x SERIES

The IGEP™ SMARC AM335x series is comprised by models with two different processor of AM335x family. All of them include WiFi/Bluetooth connectivity.

IGEP™ SMARC AM3354 is composed by an industrial AM3354 processor at speed 800 MHz, with Fast and Gigabit Ethernet and DVI output.

IGEP™ SMARC AM3352 is composed by an industrial AM3352 processor at speed 800 MHz, with Fast Ethernet.

Other combinations are available. Contact with IATEC's Sales Department for other configurations.

2.6 PARTS NUMBERS

Depending on the module configuration, the module has different parts numbers.

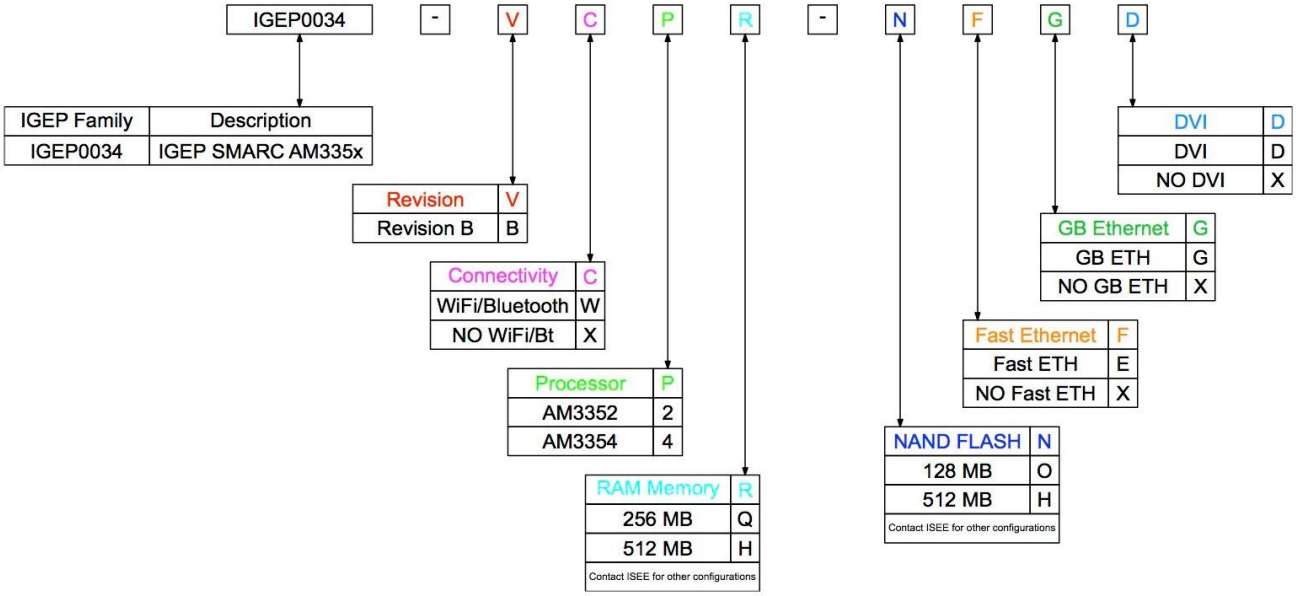


Figure 1 IGEP™ SMARC AM335x Possible Part Number

Part Number	IGEP™ Device	Description
IGEP0034-BW4H-HEGV	SMARC AM3354 WiFi	Processor: AM3354 RAM Memory: DDR3 512 MB Flash Memory: NAND 512 MB 1 x Fast Ethernet 1 x GB Ethernet DVI Connectivity: WiFi 802.11 b/g/n / Bluetooth 4.2
IGEP0034-BW2Q-OEXX	SMARC AM3352 WiFi	Processor: AM3352 RAM Memory: DDR3 256 MB Flash Memory: NAND 128 MB 1 x Fast Ethernet Connectivity: WiFi 802.11 b/g/n / Bluetooth 4.2

Table 1 IGEP™ SMARC AM335x Ordering Information.

3 HARWARE OVERVIEW

3.1 IGEPTM SMARC AM335x

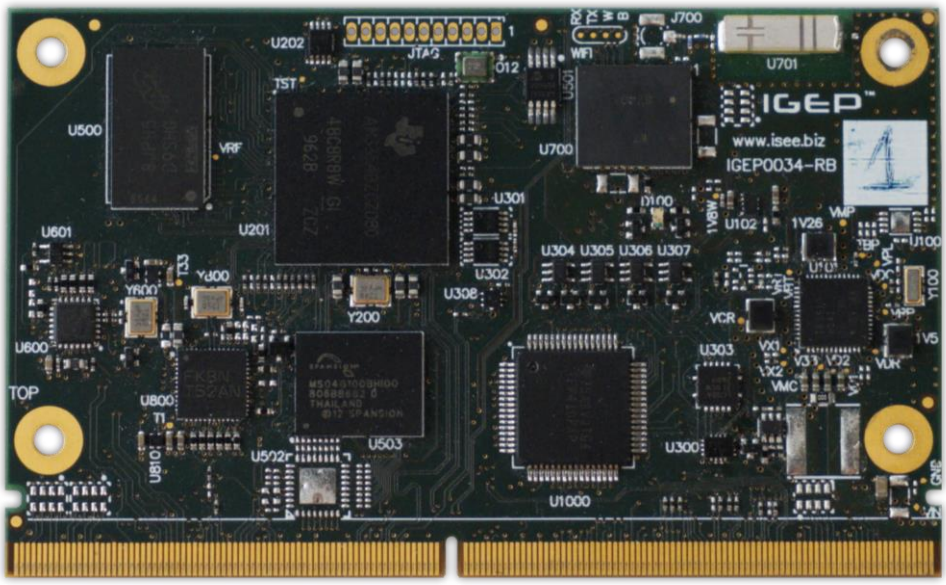


Figure 2 SMARC AM335x – Top View

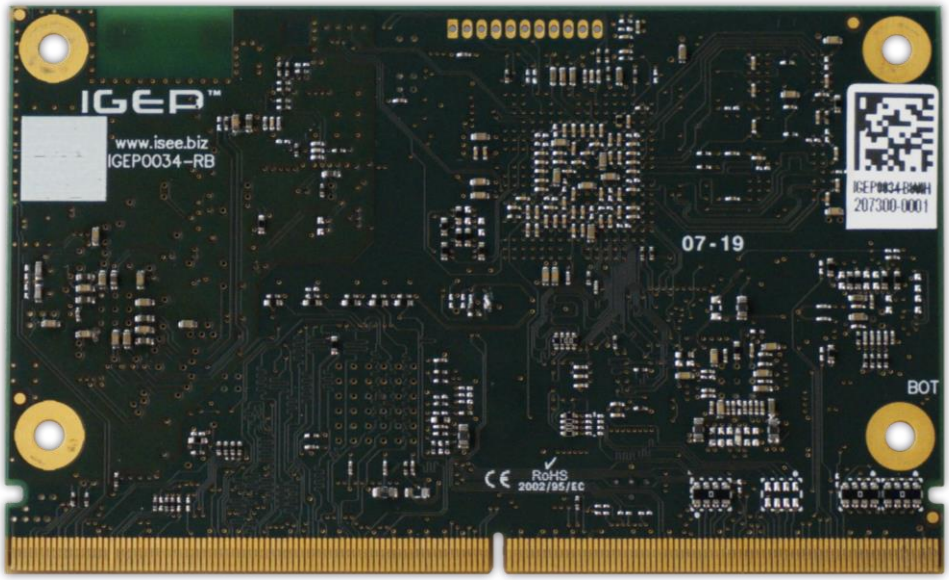


Figure 3 SMARC AM335x – Bottom View

3.2 IGEP™ SMARC AM335x BLOCK DIAGRAM

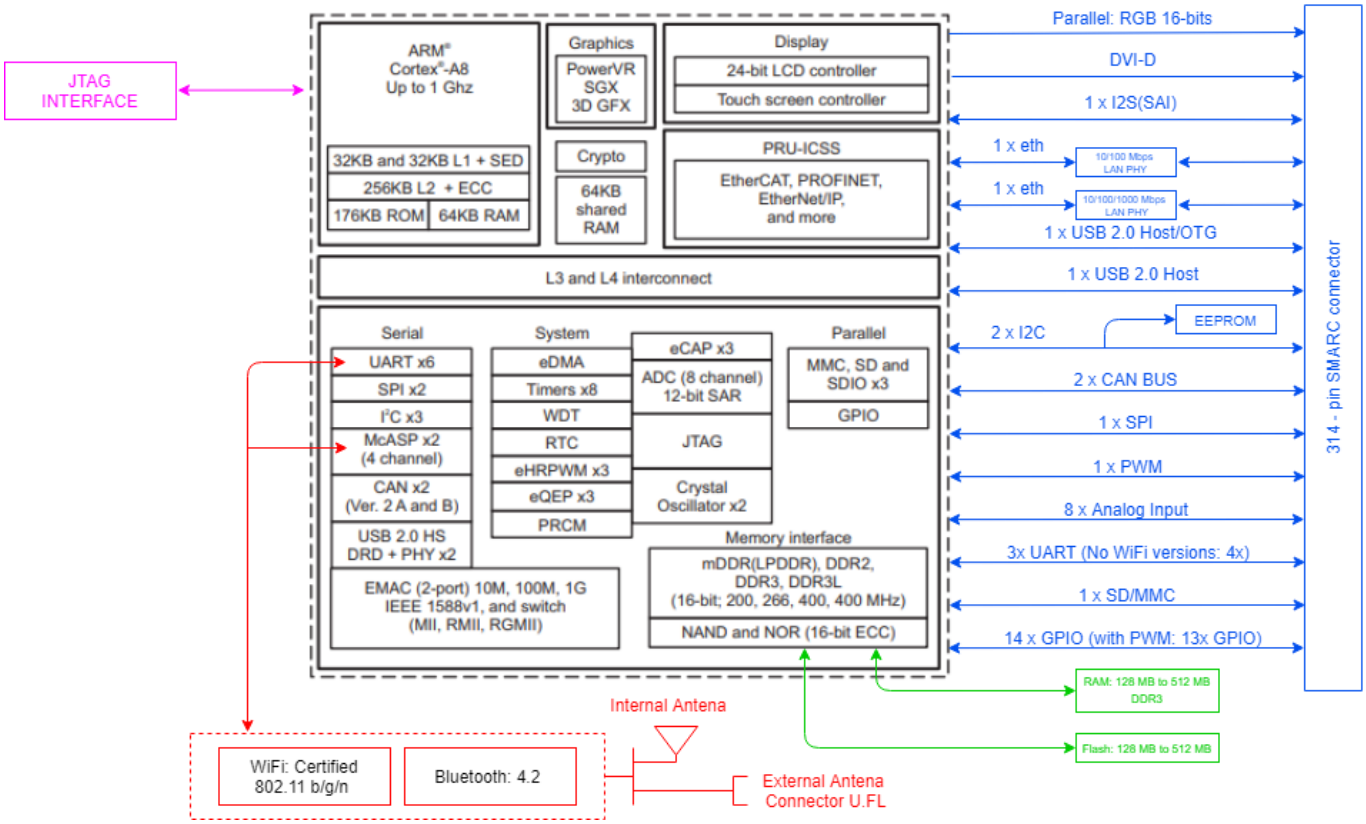


Figure 4 IGEP™ SMARC AM335x Block Diagram

3.3 IGEP™ SMARC AM335x FEATURES

Feature	Specifications
Processor	Texas Instruments AM335x ARM Cortex-A8 NEON SIMD Coprocessor Frequency: 1 GHz
Memory	RAM: 128 MB to 512 MB DDR3 Flash: 128 MB to 512 MB EEPROM: Serial I2C 32 Kb
3D/2D Graphics Accelerator	POWER VR SGX GPU, providing 2D/3D graphics acceleration. Support: Open GL ES 1.0, Open GL ES 2.0, Open VG
Video	-
Camera Interface	-
Display	Parallel: RGB 16-bits Touchscreen: On board 4 -wire Resistive + Capacitive through I2C and SPI Optional DVI-D
Digital Audio	1 x I2S(SAI)
Network	Ethernet: 1 x 10/100 Mbps with phy. Ethernet: 1x 10/100/1000 Mbps with phy. WiFi: Certified 802.11 b/g/n (Access Point: Yes) Bluetooth: 4.2
Antenna	Internal WiFi/Bluetooth antenna Optional: U.FL connector for external antenna
USB	1 x USB 2.0 Host/OTG 1 x USB 2.0 Host
External Interfaces	3x UART (No WiFi versions: 4x) 1 x SD/MMC 2x I2C 1 x SPI 14 x GPIO (with PWM: 13x GPIO) 8 x Analog Input 1 x JTAG 1 x PWM 2 x CAN BUS
OS Support	Linux Kernel 4.9 Distributions: Ubuntu 16.04, Yocto 2.3, Debian
Power Supply	Power from expansion connectors: From 4,5 V to 5,25 V Digital I/O voltage: 1,8 V
Power Consumption	0.32 A
Thermal	Industrial temperature: -40ºC to +80ºC
Form Factor	Small SMARC size: 82,00 mm x 50,00 mm
Humidity	93% relative Humidity at 40 ºC, non-condensing (according to IEC 60068-2-78)
MTBF	131400 hours (>15 years)

Table 2 On-board features

3.4 IGEP™ SMARC AM335x COMPONENTS MAP

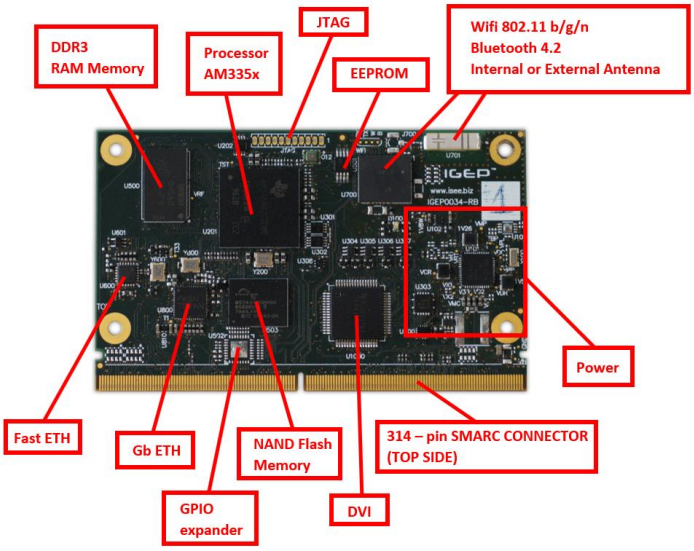


Figure 5 SMARC AM335x Components Map

3.5 TEXAS INSTRUMENTS AM335x PROCESSORS

The AM335x by Texas Instruments are a family of integrated processors based on the ARM Cortex-A8 processor with frequency speed of 1GHz (in Industrial version). They have a high performance at low cost and are delivered with 3D graphics acceleration and key peripherals. They also include industrial options (such as EtherCAT and PROFIBUS) and support different high-level operating systems (Linux and Android).

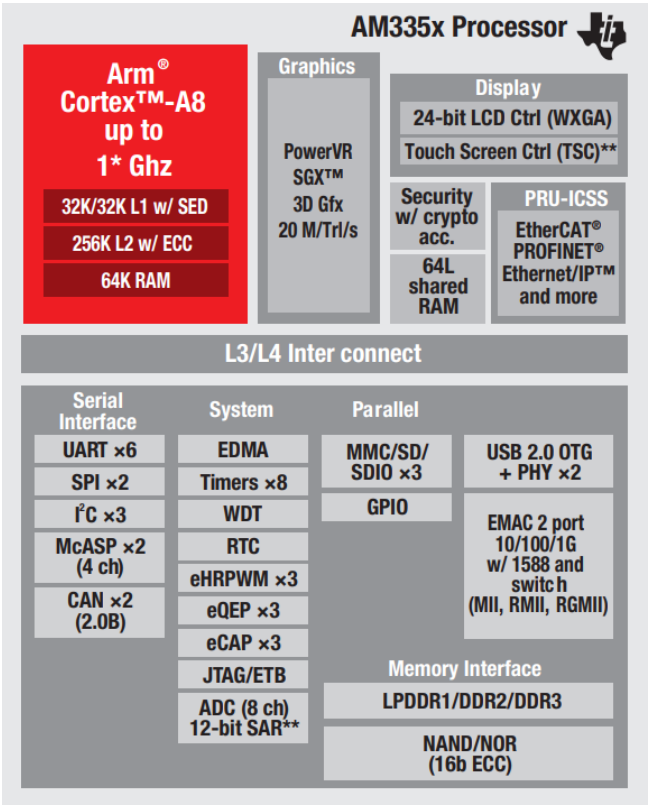


Figure 6 Texas Instruments AM335x Processors Block Diagram

4 SMARC EXPANSION CONNECTOR INTERFACE

4.1 SMARC INTERFACE DEFINITION

IGEP™ SMARC AM335x has a 314-pin SMARC interface (156 on TOP side and 158 on BOTTOM side), providing source power and 1V8 CMOS signals to support lots of AM335x processor features which could be used in custom application. The module sizes are 82mm x 50mm as the SMARC standard defines. The module pins are numbered as P1 - P156 (TOP side) and S1 - S158 (BOTTOM side).

Next figure shows the area and pin numbering of the SMARC interface.

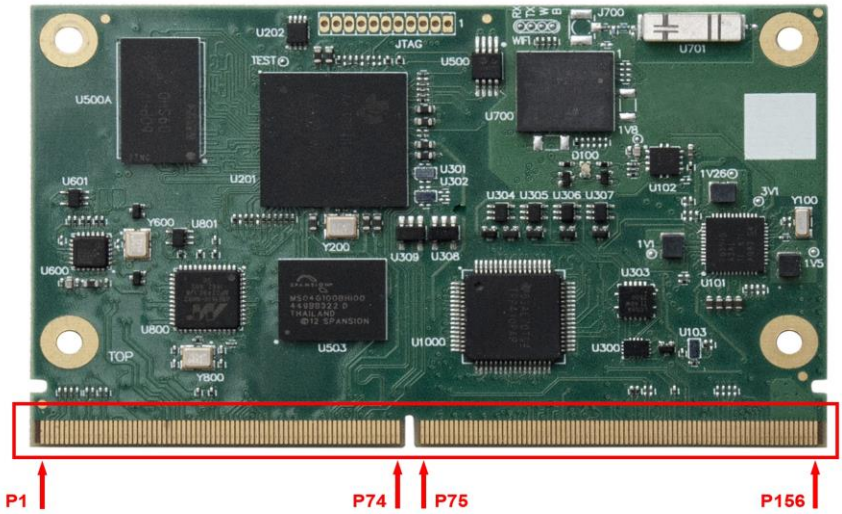


Figure 7 SMARC interface area (TOP Side)

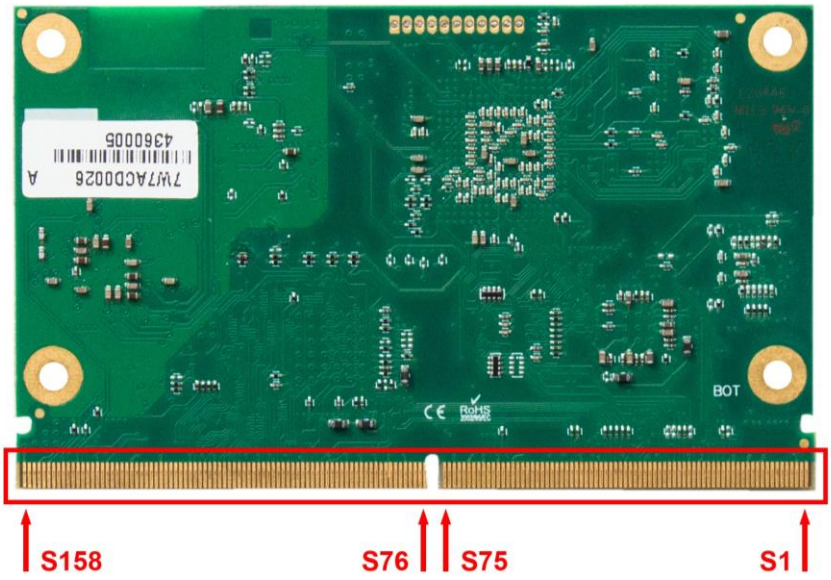


Figure 8 SMARC interface area (BOTTOM Side)

The IGEP™ SMARC AM335x modules can be inserted like a target through this SMARC interface to any of the standard connectors existing on the market. Next table shows some valid references (consult the page 73 on the SMARC 2.1 Specification to find more information).

Manufacturer	Part Number	Height
FOXCONN	AS0B821-S43B-*H	4,3 mm
FOXCONN	AS0B821-S43N-*H	4,3 mm
FOXCONN	AS0B826-S43B-*H	4,3 mm
FOXCONN	AS0B826-S43N-*H	4,3 mm
JAE	MM70-314B2-1-R500	4,3 mm
Aces	91781-314 2 8-001	5,2 mm
FOXCONN	AS0B821-S55B-*H	5,50 mm
FOXCONN	AS0B821-S55N-*H	5,50 mm
FOXCONN	AS0B826-S55B-*H	5,50 mm
FOXCONN	AS0B826-S55B-*H	5,50 mm
FOXCONN	AS0B821-S78B-*H	7,80 mm
FOXCONN	AS0B821-S78N-*H	7,80 mm
FOXCONN	AS0B826-S78B-*H	7,80 mm
FOXCONN	AS0B826-S78N-*H	7,80 mm
Yamaichi	CN113-314-2001	7,80 mm

Table 3 Valid SMARC connector part numbers

Developers must consider the SMARC connector height according to their expansion board needs.

Note: Many of the vendor drawings for the connectors listed above show a PCB footprint pattern for use with an MXM3 graphics card. This footprint, and the associated pin numbering, is not suitable for SMARC use. The MXM3 standard gangs large groups of pins together to provide ~80W capable power paths needed for X86 graphics cards.

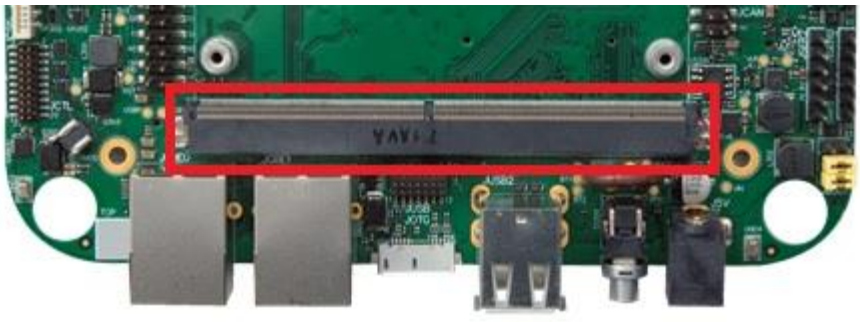


Figure 9 SMARC CONNECTOR

4.2 PINOUT TABLE OF SMARC (VERSION) EXPANSION INTERFACE

This chapter contains all the pinout details for the SMARC-314 expansion interface. The tables below show the meaning of each column in table 6, where is collected all the pins and its main functions.

COLUMN	INFORMATION PROVIDED	
PIN	Indicates the pin number of the SMARC-314 interface. It is either for Primary Side (Top Side, P#) and Secondary Side (Bottom Side, S#)	
VOLTAGE LEVEL	Signal Level Voltage	
	5V	5 V signal
	3V3	3,3 V signal
	1V8	1,8 V signal
	DS	Differential analog signaling.
	GBE MDI	Differential analog signaling for Gigabit Media Dependent Interface.
	PHY MDI	Differential analog signaling for FAST Ethernet Media Dependent Interface.
	TMDS	DVI signaling used for HDMI display interfaces.
	USB	DC coupled differential signaling used for traditional (non-Super-Speed) USB signals
	GND	Digital ground.
	RSV	Reserved.
	NC	No connected. This pin should be floating.
TYPE	Indicates pin type.	
	Power	Power signal.
	I CMOS	CMOS input pin.
	O CMOS	CMOS output pin.
	I/O CMOS	CMOS input and output pin.
	O OD CMOS	Open drain output pin.
	I/O OD CMOS	Open drain input and output pin.
	NC	No connected. This pin should be floating.
MAIN FUNCTION	Main or suggested function.	
COMMENTS	Clarification for the related SMARC-314 interface pin. See device chapter for more information.	

Table 4 SMARC expansion interface information

COLORS	INFORMATION
	Power Sources (Supply Voltages)
	Signal Level Voltage (Digital and Analog Ground)
	Control Signals
	Ethernet
	USB connections
	I2C
	SPI
	Wifi/Bluetooth and SD/SD card interface
	UART
	I2S
	CAN bus
	GPIOs
	Analog Inputs
	DVI
	LCD
	RTC Battery

Table 5 Colors Key

The following table includes all the pins and its description. Please, be careful with the name of pins related to Primary (Top side, pins PXXX) and Secondary (Bottom side, pins SXXX) sides of SMARC connector.

Pin	Volt Level	Type	Main Function	Comments
Primary (Top) Side				
P1	NC	NC	Not connected	Not connected
P2	GND	Power	GND	Digital ground
P3	1V8	Input	AIN0	Analog Input-0 (1)
P4	1V8	Input	AIN1	Analog Input-1 (1)
P5	NC	NC	Not connected	Not connected
P6	NC	NC	Not connected	Not connected
P7	1V8	Input	AIN2	Analog Input-2 (1)
P8	1V8	Input	AIN3	Analog Input-3 (1)
P9	GND	Power	GND	Digital ground
P10	1V8	Input	AIN4	Analog Input-4 (1)
P11	1V8	Input	AIN5	Analog Input-5 (1)
P12	GND	Power	GND	Digital ground
P13	1V8	Input	AIN6	Analog Input-6 (1)
P14	1V8	Input	AIN7	Analog Input-7 (1)
P15	GND	Power	GND	Digital ground
P16	NC	NC	Not connected	Not connected
P17	NC	NC	Not connected	Not connected
P18	GND	Power	GND	Digital ground
P19	NC	NC	Not connected	Not connected
P20	NC	NC	Not connected	Not connected
P21	3V3	Ouptput OD	PHY_LINK100#	FAST Ethernet Link speed indication LED for 100 Mbps. Active low.
P22	NC	NC	Not connected	Not connected
P23	NC	NC	Not connected	Not connected
P24	NC	NC	Not connected	Not connected
P25	3V3	Ouptput OD	PHY_LINK_ACT#	FAST Ethernet Link/Activity indication LED. Active low.

P26	PHY MDI	IO	PHY_RX-	FAST Ethernet pair RX to magnetics (Media Dependent Interface).
P27	PHY MDI	IO	PHY_RX+	FAST Ethernet pair RX to magnetics (Media Dependent Interface).
P28	3V3	Output	PHY_CTREF	Reference voltage for Carrier Board Ethernet magnetic.
P29	PHY MDI	IO	PHY_TX-	FAST Ethernet pair TX to magnetics (Media Dependent Interface).
P30	PHY MDI	IO	PHY_TX+	FAST Ethernet pair TX to magnetics (Media Dependent Interface).
P31	1V8	Output	SPI0_CS1#	SPI0 Interface: Master Chip Select 1. Active low.
P32	GND	Power	GND	Digital ground
P33	3V3	Input	SDIO_WP	SDIO card 4-bit Interface: Write Protect.
P34	3V3	IO	SDIO_CMD	SDIO card 4-bit Interface: Command Line.
P35	3V3	Input	SDIO_CD#	SDIO card 4-bit Interface: Card Detect.
P36	3V3	Output	SDIO_CK	SDIO card 4-bit Interface: Clock.
P37	3V3	Output	SDIO_PWR_EN	SDIO card 4-bit Interface: Card Power Enable.
P38	GND	Power	GND	Digital ground
P39	3V3	IO	SDIO_D0	SDIO card 4-bit Interface: data path (D0).
P40	3V3	IO	SDIO_D1	SDIO card 4-bit Interface: data path (D1).
P41	3V3	IO	SDIO_D2	SDIO card 4-bit Interface: data path (D2).
P42	3V3	IO	SDIO_D3	SDIO card 4-bit Interface: data path (D3).
P43	1V8	Output	SPI0_CS0#	SPI0 Interface: Master Chip Select 0. Active low.
P44	1V8	Output	SPI0_CK	SPI0 Interface: Clock.
P45	1V8	Input	SPI0_DIN	SPI0 Interface: Master Data Input.
P46	1V8	Output	SPI0_DO	SPI0 Interface: Master Data Output.
P47	GND	Power	GND	Digital ground
P48	NC	NC	Not connected	Not connected
P49	NC	NC	Not connected	Not connected
P50	GND	Power	GND	Digital ground
P51	NC	NC	Not connected	Not connected
P52	NC	NC	Not connected	Not connected
P53	GND	Power	GND	Digital ground

P54	NC	NC	Not connected	Not connected
P55	NC	NC	Not connected	Not connected
P56	NC	NC	Not connected	Not connected
P57	NC	NC	Not connected	Not connected
P58	NC	NC	Not connected	Not connected
P59	GND	Power	GND	Digital ground
P60	USB	IO	USB0+	UBS1: USB2.0 differential data input.
P61	USB	IO	USB0-	UBS1: USB2.0 differential data input.
P62	3V3	IO OD	USB0_EN_OC#	USB1: Enable (active High)-Overcurrent (active Low) PIN
P63	5V	Input	USB0_VBUS_DET	USB1: USB2.0 Host power detection when this port is used as a device.
P64	3V3	Input	USB0_OTG_ID	USB1: USB2.0 OTG ID input, active high.
P65	USB	IO	USB1+	UBS2: USB2.0/USB3.0 differential data input.
P66	USB	IO	USB1-	UBS2: USB2.0/USB3.0 differential data input.
P67	3V3	IO OD	USB1_EN_OC#	USB2: Enable OUT (active High)-Overcurrent IN(active Low) PIN
P68	GND	Power	GND	Digital ground
P69	NC	NC	Not connected	Not connected
P70	NC	NC	Not connected	Not connected
P71	NC	NC	Not connected	Not connected
P72	NC	NC	Not connected	Not connected
P73	NC	NC	Not connected	Not connected
P74	NC	NC	Not connected	Not connected
P75	NC	NC	Not connected	Not connected
P76	NC	NC	Not connected	Not connected
P77	NC	NC	Not connected	Not connected
P78	NC	NC	Not connected	Not connected
P79	GND	Power	GND	Digital ground
P80	NC	NC	Not connected	Not connected
P81	NC	NC	Not connected	Not connected
P82	GND	Power	GND	Digital ground

P83	NC	NC	Not connected	Not connected
P84	NC	NC	Not connected	Not connected
P85	GND	Power	GND	Digital ground
P86	NC	NC	Not connected	Not connected
P87	NC	NC	Not connected	Not connected
P88	GND	Power	GND	Digital ground
P89	NC	NC	Not connected	Not connected
P90	NC	NC	Not connected	Not connected
P91	GND	Power	GND	Digital ground
P92	TMDS	Output	DVI_D2+	DVI differential data output D2.
P93	TMDS	Output	DVI_D2-	DVI differential data output D2.
P94	GND	Power	GND	Digital ground
P95	TMDS	Output	DVI_D1+	DVI differential data output D1.
P96	TMDS	Output	DVI_D1-	DVI differential data output D1.
P97	GND	Power	GND	Digital ground
P98	TMDS	Output	DVI_D0+	DVI differential data output D0.
P99	TMDS	Output	DVI_D0-	DVI differential data output D0.
P100	GND	Power	GND	Digital ground
P101	TMDS	Output	DVI_CK+	DVI differential clock output pair.
P102	TMDS	Output	DVI_CK-	DVI differential clock output pair.
P103	GND	Power	GND	Digital ground
P104	NC	NC	Not connected	Not connected
P105	1V8	Output OD	HDMI_CTRL_CK	I2C2_SCL: Clock signal. Shared with IOExpander (3)
P106	1V8	IO OD	HDMI_CTRL_DAT	I2C2_SDA: Data signal. Shared with IOExpander (3)
P107	NC	NC	Not connected	Not connected
P108	1V8	IO	GPIO0	AM335x GPIO0_23
P109	1V8	IO	GPIO1	GPIO FROM IOMUX P13 (I2C2)
P110	1V8	IO	GPIO2	GPIO FROM IOMUX P14 (I2C2)
P111	1V8	IO	GPIO3	GPIO FROM IOMUX P15 (I2C2)
P112	1V8	IO	GPIO4	GPIO FROM IOMUX P16 (I2C2)

P113	1V8	IO	GPIO5-PWM	AM335x EHRPWM2A or GPIO0_22
P114	1V8	IO	GPIO6	GPIO FROM IOMUX P20 (I2C2)
P115	1V8	IO	GPIO7	GPIO FROM IOMUX P21 (I2C2)
P116	1V8	IO	GPIO8	GPIO FROM IOMUX P22(I2C2)
P117	1V8	IO	GPIO9	GPIO FROM IOMUX P23 (I2C2)
P118	1V8	IO	GPIO10	GPIO FROM IOMUX P24 (I2C2)
P119	1V8	IO	GPI11	GPIO FROM IOMUX P25 (I2C2)
P120	GND	Power	GND	Digital ground
P121	1V8	O OD	I2C_PM_CK	I2C1_SCL: Clock signal. PMIC & EEPROM shared
P122	1V8	IO OD	I2C_PM_DAT	I2C1_SDA: Data signal. PMIC & EEPROM shared
P123	1V8	Input	BOOT_SEL0#	Boot device. Active Low.
P124	1V8	Input	BOOT_SEL1#	Boot device. Active Low.
P125	1V8	Input	BOOT_SEL2#	Boot device. Active Low.
P126	1V8	Output	RESET_OUT#	Reset out to Carrier. Active Low. nRESPWRON PIN of PMIC
P127	1V8	Input	RESET_IN#	Reset input from Carrier. Active Low. Connected to PORZ
P128	1V8	Input	POWER_BTN#	Power button input. Active Low. Connected to PMIC PWRON
P129	1V8	Output	SER0_TX	UART3_TX: Asynchronous serial port 1 data out.
P130	1V8	Input	SER0_RX	UART3_RX: Asynchronous serial port 1 data in.
P131	NC	NC	Not connected	Not connected
P132	NC	NC	Not connected	Not connected
P133	GND	Power	GND	Digital ground
P134	1V8	Output	SER1_TX	UART0_TX: Asynchronous serial port 1 data out.
P135	1V8	Input	SER1_RX	UART0_RX: Asynchronous serial port 1 data in.
P136	1V8	Output	SER2_TX	UART2_TX: Asynchronous serial port 1 data out. (2)
P137	1V8	Input	SER2_RX	UART2_RX: Asynchronous serial port 1 data in. (2)
P138	1V8	Output	SER2_RTS#	UART2_RTS: Request to Send handshake line. Active low. (2)
P139	1V8	Input	SER2_CTS#	UART2_CTS: Clear to Send handshake line. Active low. (2)
P140	1V8	Output	SER3_TX	UART5_TX: Asynchronous serial port 1 data out.

P141	1V8	Input	SER3_RX	UART5_RX: Asynchronous serial port 1 data in.
P142	GND	Power	GND	Digital ground
P143	1V8	Output	CAN0_TX	CAN0_TX
P144	1V8	Input	CAN0_RX	CAN0_RX
P145	1V8	Output	CAN1_TX	CAN1_TX
P146	1V8	Input	CAN1_RX	CAN1_RX
P147	5V	Power	VDD_IN	Pins used to power up the module. [4,50 V to 5,25 V]
P148	5V	Power	VDD_IN	Pins used to power up the module. [4,50 V to 5,25 V]
P149	5V	Power	VDD_IN	Pins used to power up the module. [4,50 V to 5,25 V]
P150	5V	Power	VDD_IN	Pins used to power up the module. [4,50 V to 5,25 V]
P151	5V	Power	VDD_IN	Pins used to power up the module. [4,50 V to 5,25 V]
P152	5V	Power	VDD_IN	Pins used to power up the module. [4,50 V to 5,25 V]
P153	5V	Power	VDD_IN	Pins used to power up the module. [4,50 V to 5,25 V]
P154	5V	Power	VDD_IN	Pins used to power up the module. [4,50 V to 5,25 V]
P155	5V	Power	VDD_IN	Pins used to power up the module. [4,50 V to 5,25 V]
P156	5V	Power	VDD_IN	Pins used to power up the module. [4,50 V to 5,25 V]
Secondary (Bottom) Side				
S1	NC	NC	Not connected	Not connected
S2	NC	NC	Not connected	Not connected
S3	GND	Power	GND	Digital ground
S4	NC	NC	Not connected	Not connected
S5	NC	NC	Not connected	Not connected
S6	NC	NC	Not connected	Not connected
S7	NC	NC	Not connected	Not connected
S8	NC	NC	Not connected	Not connected
S9	NC	NC	Not connected	Not connected
S10	GND	Power	GND	Digital ground
S11	NC	NC	Not connected	Not connected
S12	NC	NC	Not connected	Not connected
S13	GND	Power	GND	Digital ground
S14	NC	NC	Not connected	Not connected

S15	NC	NC	Not connected	Not connected
S16	GND	Power	GND	Digital ground
S17	GBE MDI	IO	GBE1_MDI0+	GB Ethernet pair 0 to magnetics (Media Dependent Interface).
S18	GBE MDI	IO	GBE1_MDI0-	GB Ethernet pair 0 to magnetics (Media Dependent Interface).
S19	3V3	Ouptput OD	GBE1_LINK100	GB Ethernet Link speed indication LED for 100 Mbps. Active low.
S20	GBE MDI	IO	GBE1_MDI1+	GB Ethernet pair 1 to magnetics (Media Dependent Interface).
S21	GBE MDI	IO	GBE1_MDI1-	GB Ethernet pair 1 to magnetics (Media Dependent Interface).
S22	NC	NC	Not connected	Not connected
S23	GBE MDI	IO	GBE1_MDI2+	GB Ethernet pair 2 to magnetics (Media Dependent Interface).
S24	GBE MDI	IO	GBE1_MDI2-	GB Ethernet pair 2 to magnetics (Media Dependent Interface).
S25	GND	Power	GND	Digital ground
S26	GBE MDI	IO	GBE1_MDI3+	GB Ethernet pair 3 to magnetics (Media Dependent Interface).
S27	GBE MDI	IO	GBE1_MDI3-	GB Ethernet pair 3 to magnetics (Media Dependent Interface).
S28	2V5	Power	GBE1_CTREF	Reference voltage for Carrier Board Ethernet magnetic.
S29	NC	NC	Not connected	Not connected
S30	NC	NC	Not connected	Not connected
S31	3V3	Ouptput OD	GBE1_LINK_ACT#	GB Ethernet Link/Activity indication LED. Active low.
S32	NC	NC	Not connected	Not connected
S33	NC	NC	Not connected	Not connected
S34	GND	Power	GND	Digital ground
S35	1V8	IO	GPIO	GPIO1_30
S36	1V8	IO	GPIO	GPIO1_31
S37	NC	NC	Not connected	Not connected
S38	1V8	Output	AUDIO_MCK	I2S: Master Clock output to Audio codecs. 12MHz CLOCK.
S39	1V8	IO	I2S0_LRCK	MCASP0_FSX: Left & Right Audio Frame synchronization clock.
S40	1V8	Output	I2S0_SDOUT	MCASP0_AXR0: Digital Audio output.
S41	1V8	Input	I2S0_SDIN	MCASP0_AXR1: Digital Audio input.

S42	1V8	IO	I2S0_CK	MCASP0_ACLKX: Digital Audio clock.
S43	NC	NC	Not connected	Not connected
S44	NC	NC	Not connected	Not connected
S45	NC	NC	Not connected	Not connected
S46	NC	NC	Not connected	Not connected
S47	GND	Power	GND	Digital ground
S48	1V8	IO OD	I2C_GP_CK	I2C1_SCL: Clock signal. PMIC & EEPROM shared
S49	1V8	IO OD	I2C_GP_DAT	I2C1_SDA: Data signal. PMIC & EEPROM shared
S50	NC	NC	Not connected	Not connected
S51	NC	NC	Not connected	Not connected
S52	NC	NC	Not connected	Not connected
S53	NC	NC	Not connected	Not connected
S54	NC	NC	Not connected	Not connected
S55	NC	NC	Not connected	Not connected
S56	NC	NC	Not connected	Not connected
S57	NC	NC	Not connected	Not connected
S58	NC	NC	Not connected	Not connected
S59	NC	NC	Not connected	Not connected
S60	NC	NC	Not connected	Not connected
S61	GND	Power	GND	Digital ground
S62	NC	NC	Not connected	Not connected
S63	NC	NC	Not connected	Not connected
S64	GND	Power	GND	Digital ground
S65	NC	NC	Not connected	Not connected
S66	NC	NC	Not connected	Not connected
S67	GND	Power	GND	Digital ground
S68	NC	NC	Not connected	Not connected
S69	NC	NC	Not connected	Not connected
S70	GND	Power	GND	Digital ground
S71	NC	NC	Not connected	Not connected
S72	NC	NC	Not connected	Not connected
S73	GND	Power	GND	Digital ground

S74	NC	NC	Not connected	Not connected
S75	NC	NC	Not connected	Not connected
S76	GND	Analog	GND_ADC	Analog Ground. Ground reference for ADC analog inputs.
S77	1V8	Power	VREFP_ADC	1,8Volt reference voltage for ADC analog inputs
S78	NC	NC	Not connected	Not connected
S79	NC	NC	Not connected	Not connected
S80	GND	Power	GND	Digital ground
S81	NC	NC	Not connected	Not connected
S82	NC	NC	Not connected	Not connected
S83	GND	Power	GND	Digital ground
S84	NC	NC	Not connected	Not connected
S85	NC	NC	Not connected	Not connected
S86	GND	Power	GND	Digital ground
S87	NC	NC	Not connected	Not connected
S88	NC	NC	Not connected	Not connected
S89	GND	Power	GND	Digital ground
S90	NC	NC	Not connected	Not connected
S91	NC	NC	Not connected	Not connected
S92	GND	Power	GND	Digital ground
S93	NC	NC	Not connected	Not connected
S94	NC	NC	Not connected	Not connected
S95	NC	NC	Not connected	Not connected
S96	1V8	Output	LCD_D0	LCD_DATA0 (Blue0)
S97	1V8	Output	LCD_D1	LCD_DATA1 (Blue1)
S98	1V8	Output	LCD_D2	LCD_DATA2 (Blue2)
S99	1V8	Output	LCD_D3	LCD_DATA3 (Blue3)
S100	1V8	Output	LCD_D4	LCD_DATA4 (Blue4)
S101	GND	Power	GND	Digital ground
S102	NC	NC	Not connected	Not connected
S103	NC	NC	Not connected	Not connected
S104	1V8	Output	LCD_D5	LCD_DATA5 (Green0)
S105	1V8	Output	LCD_D6	LCD_DATA6 (Green1)

S106	1V8	Output	LCD_D7	LCD_DATA7 (Green2)
S107	1V8	Output	LCD_D8	LCD_DATA8 (Green3)
S108	1V8	Output	LCD_D9	LCD_DATA9 (Green4)
S109	1V8	Output	LCD_D10	LCD_DATA10 (Green5)
S110	GND	Power	GND	Digital ground
S111	NC	NC	Not connected	Not connected
S112	NC	NC	Not connected	Not connected
S113	NC	NC	Not connected	Not connected
S114	1V8	Output	LCD_D11	LCD_DATA11 (Red0)
S115	1V8	Output	LCD_D12	LCD_DATA12 (Red1)
S116	1V8	Output	LCD_D13	LCD_DATA13 (Red2)
S117	1V8	Output	LCD_D14	LCD_DATA14 (Red3)
S118	1V8	Output	LCD_D15	LCD_DATA15 (Red4)
S119	GND	Power	GND	Digital ground
S120	1V8	Output	LCD_DE	LCD_AC_BIAS_ENABLE
S121	1V8	Output	LCD_VS	LCD_VSYNC
S122	1V8	Output	LCD_HS	LCD_HSYNC
S123	1V8	Output	LCD_PCK	LCD_CLK
S124	GND	Power	GND	Digital ground
S125	NC	NC	Not connected	Not connected
S126	NC	NC	Not connected	Not connected
S127	1V8	Output	LCD_BKLT_EN	GPIO FROM IOMUX P27 (I2C2) LCD Panel Backlite Enable
S128	NC	NC	Not connected	Not connected
S129	NC	NC	Not connected	Not connected
S130	NC	NC	Not connected	Not connected
S131	NC	NC	Not connected	Not connected
S132	NC	NC	Not connected	Not connected
S133	1V8	Output	LCD_VDD_EN	GPIO FROM IOMUX P26 (I2C2) LCD Panel Power Enable
S134	NC	NC	Not connected	Not connected
S135	NC	NC	Not connected	Not connected
S136	GND	Power	GND	Digital ground

S137	NC	NC	Not connected	Not connected
S138	NC	NC	Not connected	Not connected
S139	1V8	IO OD	I2C_LCD_CK	I2C2_SCL: Clock signal. Shared with IOExpander
S140	1V8	IO OD	I2C_LCD_DAT	I2C2_SDA: Data signal. Shared with IOExpander
S141	1V8	Output	LCD_BKLT_PWM	LCD Panel Backlite PWM signal EHRPWM2A or GPIO0_22
S142	NC	NC	Not connected	Not connected
S143	GND	Power	GND	Digital ground
S144	NC	NC	Not connected	Not connected
S145	NC	NC	Not connected	Not connected
S146	1V8	Input	WAKEUP	Wakeup signal from Carrier to microprocessor
S147	3V0	Power	VDD_RTC	Coin Cell Battery input for RTC [3,0Volts]
S148	NC	NC	Not connected	Not connected
S149	1V8	Input	SLEEP	Sleep signal from Carrier to PMIC
S150	1V8	Output	PMIC_PWR_EN	PMIC Power Enable signal from microprocessor to PMIC and optionally to Carrier
S151	NC	NC	Not connected	Not connected
S152	NC	NC	Not connected	Not connected
S153	1V8	Output	CARRIER_STBY#	Carrier Standby signal [GPIO FROM IOMUX P02 (I2C2)] from module to Carrier
S154	1V8	Output	CARRIER_PWR_ ON#	Carrier Power ON signal to Carrier goes to GPIO IOMUX P03 (I2C2)
S155	1V8	Input	FORCE RECOVERY#	Recovery signal from Carrier to boot from serial Downloader
S156	NC	NC	Not connected	Not connected
S157	NC	NC	Not connected	Not connected
S158	GND	Power	GND	Digital ground
Notes				
(1)	Unprotected. Maximum 1,8 V			
(2)	This function is only present in No WiFi models.			
(3)	I2C Clock and Data lines for HDMI.			

Table 6 SMARC pinout description

5 PRODUCT SPECIFICATIONSUMMARY

5.1 POWER SOURCES

5.1.1 Supply Voltage

The power supply of the module is made with a single standard voltage of 5V, using the defined inputs (pins P147 to P156, all the connections in this chapter are referred to the SMARC-314 connector, see Table 7 Power Supply pins). This voltage can be from a minimum value of 4.5V to a maximum of 5.5V (see resume of electrical characteristics in Chapter 7: ELECTRICAL CHARACTERISTICS). Next figure shows a schematic example of this power signal (page 88 of SMARC Design Guide).

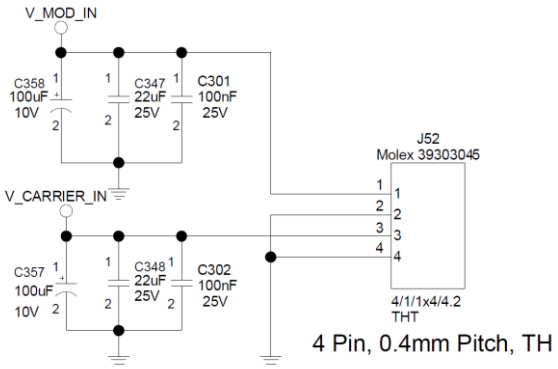


Figure 10 Power Supply Input circuit

Pin	Volt Level	Type	Main Function	Comments
5V Input Power				
P147	5V	Power	VDD_IN0	Pins used to power up the module. Source voltage should be between 4V5 to 5V25
P148	5V	Power	VDD_IN1	Pins used to power up the module. Source voltage should be between 4V5 to 5V25
P149	5V	Power	VDD_IN2	Pins used to power up the module. Source voltage should be between 4V5 to 5V25
P150	5V	Power	VDD_IN3	Pins used to power up the module. Source voltage should be between 4V5 to 5V25
P151	5V	Power	VDD_IN4	Pins used to power up the module. Source voltage should be between 4V5 to 5V25
P152	5V	Power	VDD_IN5	Pins used to power up the module. Source voltage should be between 4V5 to 5V25
P153	5V	Power	VDD_IN6	Pins used to power up the module. Source voltage should be between 4V5 to 5V25
P154	5V	Power	VDD_IN7	Pins used to power up the module. Source voltage should be between 4V5 to 5V25
P155	5V	Power	VDD_IN8	Pins used to power up the module. Source voltage should be between 4V5 to 5V25
P156	5V	Power	VDD_IN9	Pins used to power up the module. Source voltage should be between 4V5 to 5V25
1V8 Analog Reference				
S77	1V8	Power	VREFP_ADC	1,8Volt reference voltage for ADC analog inputs

Table 7 Power Supply pins

5.1.2 Digital and Analog Ground

All the GND pins are internally connected, so it is not needed to connect all of them. However, the user has to considerer how many of them connect according to the total consumption of the complete circuit (the IGEP™ SMARC AM335x and the base board developed). At the same time, to make the routing of buses easier, the ground connection chosen will be the nearest to the function used.

Pin	Volt Level	Type	Main Function	Comments
Digital Ground				
P2	GND	Power	GND	Digital ground
P9	GND	Power	GND	Digital ground
P12	GND	Power	GND	Digital ground
P15	GND	Power	GND	Digital ground
P18	GND	Power	GND	Digital ground
P32	GND	Power	GND	Digital ground
P38	GND	Power	GND	Digital ground
P47	GND	Power	GND	Digital ground
P50	GND	Power	GND	Digital ground
P53	GND	Power	GND	Digital ground
P59	GND	Power	GND	Digital ground
P68	GND	Power	GND	Digital ground
P79	GND	Power	GND	Digital ground
P82	GND	Power	GND	Digital ground
P85	GND	Power	GND	Digital ground
P88	GND	Power	GND	Digital ground
P91	GND	Power	GND	Digital ground
P94	GND	Power	GND	Digital ground
P97	GND	Power	GND	Digital ground
P100	GND	Power	GND	Digital ground
P103	GND	Power	GND	Digital ground
P120	GND	Power	GND	Digital ground
P133	GND	Power	GND	Digital ground
P142	GND	Power	GND	Digital ground

S3	GND	Power	GND	Digital ground
S10	GND	Power	GND	Digital ground
S13	GND	Power	GND	Digital ground
S16	GND	Power	GND	Digital ground
S25	GND	Power	GND	Digital ground
S34	GND	Power	GND	Digital ground
S47	GND	Power	GND	Digital ground
S61	GND	Power	GND	Digital ground
S64	GND	Power	GND	Digital ground
S67	GND	Power	GND	Digital ground
S70	GND	Power	GND	Digital ground
S73	GND	Power	GND	Digital ground
S76	GND	Analog	GND_ADC	Analog Ground. Ground reference for ADC analog inputs.
S80	GND	Power	GND	Digital ground
S83	GND	Power	GND	Digital ground
S86	GND	Power	GND	Digital ground
S89	GND	Power	GND	Digital ground
S92	GND	Power	GND	Digital ground
S101	GND	Power	GND	Digital ground
S110	GND	Power	GND	Digital ground
S119	GND	Power	GND	Digital ground
S124	GND	Power	GND	Digital ground
S136	GND	Power	GND	Digital ground
S143	GND	Power	GND	Digital ground
S158	GND	Power	GND	Digital ground

Table 8 Digital and Analog Ground pins

5.2 CONTROL SIGNALS

There are different pins used as general control signals. They affect the *Boot Mode*, the management of the power supply and resets.

Boot Mode

The Boot Mode can be fixed by user acting over the pins P125, P124 and P123. When the module is powered on, it reads these pins, and it boots as it is specified in next table.

BOOT_SEL2# (P125)	BOOT_SEL2# (P124)	BOOT_SEL2# (P123)	Boot source
GND	GND	GND	Reserved
GND	GND	Float	Carrier SD Card
GND	Float	GND	Carrier eMMC Flash
GND	Float	Float	Carrier SPI
Float	GND	GND	Module device
Float	GND	Float	Remote boot
Float	Float	GND	Reserved
Float	Float	Float	Reserved

Table 9 Boot Mode

Reserved positions are combinations which are not implemented in current SMARC module. Users must avoid using them since it would not be possible to complete a module boot up.

Please, be careful that **default position is '111'.** This is a reserved position, and it is not possible to perform a complete module boot up since there is not an implemented Flash-SPI at Boot instructions. The User must use any of available combinations. In example, it is possible to boot from a SD-Card using combination '001'.

It is recommended to use a jumper header or a switch in series with a low resistor value (as a short circuit protector element) tied to GND in Carrier Board to control the values of these boot pins as it is showed in next figure (page 29 of SMARC Design Guide).

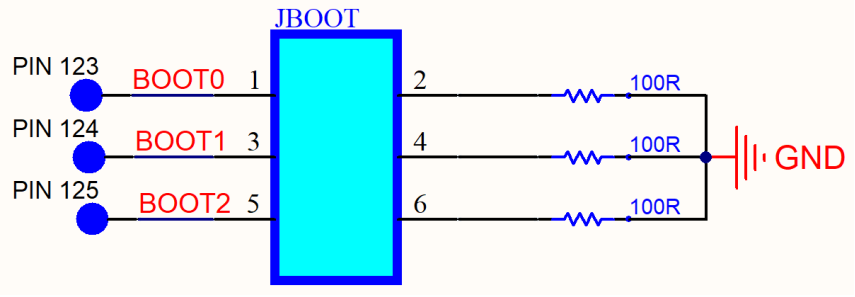


Figure 11 Boot Mode: jumpers selectors

5.2.1 Reset pins

There are two available Reset pins in the module for general purposes.

- **RESET_OUT# (P126)** - General purpose reset output to Carrier Board, active Low. Related to pin nRESPWRON of PMIC (TPS65910A3A1RSL, pin 40).
- **RESET_IN# (P127)** - Reset input from Carrier Board, active Low. Connected to PORZ (processor ball B15).

5.2.2 External Pushbutton

- **Power-button input**

POWER_BTN# (P128) - Power-button input from Carrier board, active Low. Connected to pin PWRON (PMIC pin 33).

5.2.3 Module State Pins

- **Wake Up**

WAKEUP (S146) - Wakeup signal from Carrier to processor. Connected to EXT_WAKEUP (processor ball C5).

- **Sleep**

SLEEP (S149) - Sleep signal from Carrier to PMIC. Connected to SLEEP (PMIC pin 37).

- **PMIC Power Enable**

PMIC_PWR_EN (S150) - PMIC Power Enable signal from Processor to PMIC and, optionally, to Carrier board.

- **Carrier Standby**

CARRIER_STBY# (S153) - Carrier Standby signal, send from module to Carrier. Connected to P02 of GPIO expander (TCA6424ARGJT pin 3).

- **Carrier Power On**

CARRIER_PWR_ON# (S154) - Carrier Power ON signal to Carrier. Connected to P03 (GPIO expander pin 4). Connected to PMIC_POWER_EN (processor ball C6).

- **Force Recovery**

FORCE_RECOV# (S155) - Recovery signal from Carrier board to Boot from serial Downloader. Connected to Boot decoder (SN74LVC138ARSVR).

The table below shows a summary of all control signals:

Pin	Volt Level	Type	Main Function	Comments
BOOT MODES				
P123	1V8	Input	BOOT_SEL0#	Boot device. Active Low.
P124	1V8	Input	BOOT_SEL1#	Boot device. Active Low.
P125	1V8	Input	BOOT_SEL2#	Boot device. Active Low.
RESET PINS				
P126	1V8	Output	RESET_OUT#	Reset out to Carrier. Active Low. nRESPWRON PIN of PMIC.
P127	1V8	Input	RESET_IN#	Reset input from Carrier. Active Low. Connected to PORZ.

OTHER PINS				
P128	1V8	Input	POWER_BTN#	Power button input. Active Low. Connected to PMIC PWRON.
S146	1V8	Input	WAKEUP	Wakeup signal from Carrier to microprocessor.
S149	1V8	Input	SLEEP	Sleep signal from Carrier to PMIC.
S150	1V8	Output	PMIC_PWR_EN	PMIC Power Enable signal from microprocessor to PMIC and optionally to Carrier.
S153	1V8	Output	CARRIER_STBY#	Carrier Standby signal [GPIO FROM IOMUX P02 (I2C2)] from module to Carrier.
S154	1V8	Output	CARRIER_PWR_ON#	Carrier Power ON signal to Carrier goes to GPIO IOMUX P03 (I2C2).
S155	1V8	Input	FORCE_RECOVERY#	Recovery signal from Carrier to boot from serial Downloader.

Table 10 Control Signals pins

5.3 ETHERNET

There are two Ethernet ports in the SMARC AM335x module: one Fast Ethernet (10/100 Mbps) and one Gigabit Ethernet (10/100/1000 Mbps). Both have implemented a physical layer and a block of pins of SMARC-314 interface that can be connected directly to the Ethernet LAN. Both transmission and reception lines (TX and RX) are differential (with pin function indicated as Negative and Positive) and **they should be connected to isolation magnetics**. The data lines have to be equal length and symmetric, and respect a 100 Ω differential impedance in the layout traces. The differential pairs must be isolated from nearby signals and circuitry to maintain the signal integrity.

Moreover, the magnetics module has a critical effect, so it has to be designed carefully. In order to obtain a smaller size, it is usual to use RJ45 connectors with the magnetics incorporated. If the magnetics are discrete components, they have to respect a separation under of 25 mm between them and the RJ45 connector, and 20 mm or greater between them and the SMARC-314 connector.

Fast Ethernet

According to previous comment, there is implemented a physical layer (PHY) which allows a connector that can be connected directly to the Ethernet LAN. Key benefits of PHY used are next:

- Compliant with IEEE802.3/802.3u (Fast Ethernet).
- Compliant with ISO 802-3/IEEE 802.3 (10BASE-T).
- Loop-back modes.
- Auto-negotiation.
- Automatic polarity detection and correction.
- Link status change wake-up detection.
- Vendor specific register functions.
- Supports the reduced pin count RMII interface.

The Fast Ethernet port uses two differential pairs, and they should be connected to isolation magnetics.

There is also possible to connect two LEDs to indicate the good functionning of the Ethernet connection. The first one (PHY_LINK_ACT#) indicates the line activity (LED on indicates a valid link; LED blinking when there is data traffic). The second one (PHY_LINK100#) is a link speed indication for 100 Mbps. There are usually in green and yellow color (respectively for Activity and Speed).

A last used pin is PHY_CTREF. This is to be used as reference voltage for Carrier Board Ethernet magnetic (if it is required by the module PHY).

Resistor used for LINK connectivity is **220 ohms.**

Gigabit Ethernet

- There is an additional port supporting Gigabit Ethernet (10/100/1000 Mbps). It also has implemented a physical layer (PHY) to be connected directly to the Ethernet LAN. Key benefits of PHY used are next:
- Compliant with IEEE802.3 (10BASE-T, 100BASE-T and 1000BASE-T) specifications.
- Supports RGMII, RMII
- Supports 1,5 V, 1,8 V, 2,5 V and 3,3 V CMOS for RGMII versions 1.3 and 2.0 (without HSTL support), as well as RMII version 1.2
- Supports a variety of clock sources: 25 MHz Xtal, 25 MHz OSC, 125 MHz OSC
- Supports programmable output frequencies of 25 MHz, 50 MHz or 125 MHz, regardless of chosen Xtal or OSC frequencies.
- Supports a wide array of stand-alone hardware configuration options.
- Supports all 5 bits of MDIO/MDC addressing possible for managed mode designs using pull-up/pull-down resistors.
- Devices support operating temperatures of -40ºC ambient to 125ºC junction or 0ºC ambient to 125ºC junction.
- Optionally reports if a link partner is requesting inline Power-over-Ethernet (PoE and PoE+)
- Available in 6 mm x 6 mm, 48-pin QFN package.

In the next figure (page 69 of SMARC Design Guide) is shown an example of connection diagram, using a RJ45 connector with integrated magnetics.

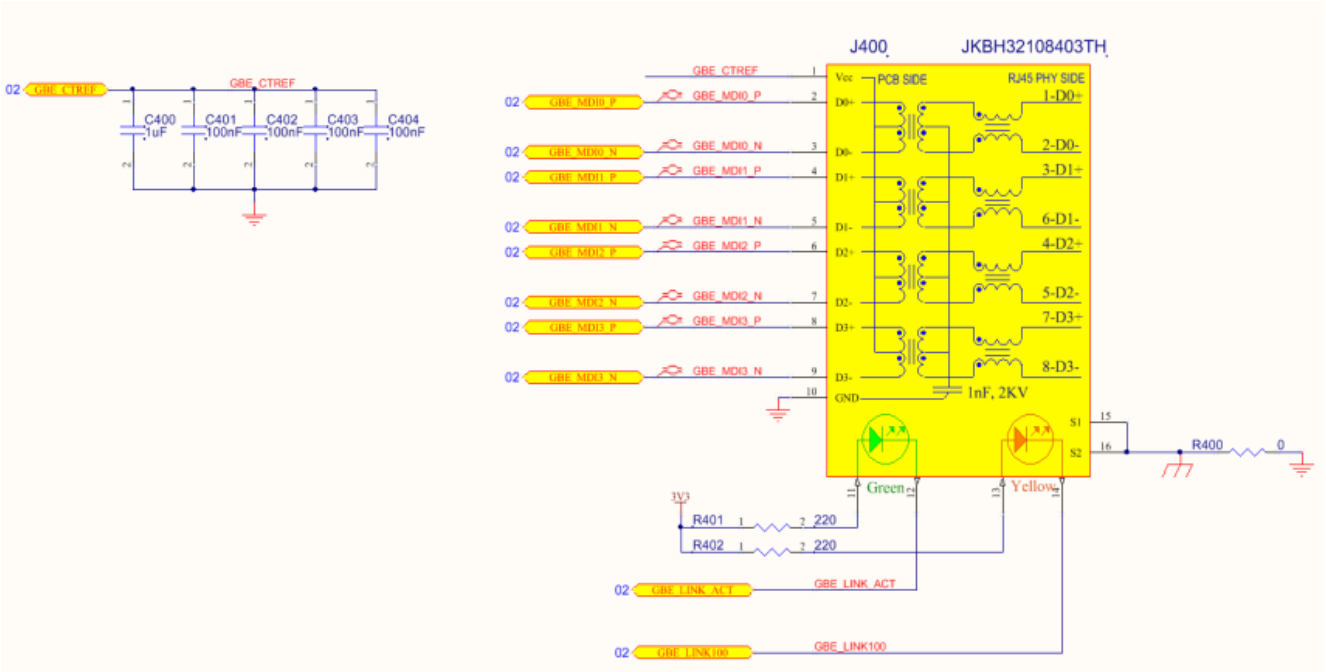


Figure 12 Ethernet 10/100/1000 Mbps standard circuit

The following table presents all the Ethernet pins:

Pin	Volt Level	Type	Main Function	Comments
ETHERNET 1				
P21	3V3	Output OD	PHY_LINK100#	FAST Ethernet Link speed indication LED for 100 Mbps. Active low.
P25	3V3	Output OD	PHY_LINK_ACT#	FAST Ethernet Link/Activity indication LED. Active low.
P26	PHY MDI	IO	PHY_RX-	FAST Ethernet pair RX to magnetics (Media Dependent Interface).
P27	PHY MDI	IO	PHY_RX+	FAST Ethernet pair RX to magnetics (Media Dependent Interface).
P28	3V3	Output OD	PHY_CTREF	Reference voltage for Carrier Board Ethernet magnetic.
P29	PHY MDI	IO	PHY_TX-	FAST Ethernet pair TX to magnetics (Media Dependent Interface).
P30	PHY MDI	IO	PHY_TX+	FAST Ethernet pair TX to magnetics (Media Dependent Interface).
ETHERNET 2				
S17	GBE MDI	IO	GBE1_MDI0+	GB Ethernet pair 0 to magnetics (Media Dependent Interface).
S18	GBE MDI	IO	GBE1_MDI0-	GB Ethernet pair 0 to magnetics (Media Dependent Interface).
S19	3V3	Output OD	GBE1_LINK100	GB Ethernet Link speed indication LED for 100 Mbps. Active low.
S20	GBE MDI	IO	GBE1_MDI1+	GB Ethernet pair 1 to magnetics (Media Dependent Interface).
S21	GBE MDI	IO	GBE1_MDI1-	GB Ethernet pair 1 to magnetics (Media Dependent Interface).
S23	GBE MDI	IO	GBE1_MDI2+	GB Ethernet pair 2 to magnetics (Media Dependent Interface).
S24	GBE MDI	IO	GBE1_MDI2-	GB Ethernet pair 2 to magnetics (Media Dependent Interface).
S26	GBE MDI	IO	GBE1_MDI3+	GB Ethernet pair 3 to magnetics (Media Dependent Interface).
S27	GBE MDI	IO	GBE1_MDI3-	GB Ethernet pair 3 to magnetics (Media Dependent Interface).
S28	2V5	Power	GBE1_CTREF	Reference voltage for Carrier Board Ethernet magnetic.
S31	3V3	Output OD	GBE1_LINK_ACT#	GB Ethernet Link/Activity indication LED. Active low.

Table 11 Ethernet 10/100/1000 Mbps pins

5.4 USB CONNECTIONS

There are two possibilities to connect the module to other USB devices: with a standard Host base and with an OTG (On-The-Go) interface.

The USB 2.0 Host connection is provided for connecting other devices acting as Clients of the module (for example, an external HDD). The SMARC-314 connector lines referred to this function are adapted for a USB type A receptacle, see wiring example in the next figure (page 65 of SMARC Design Guide).

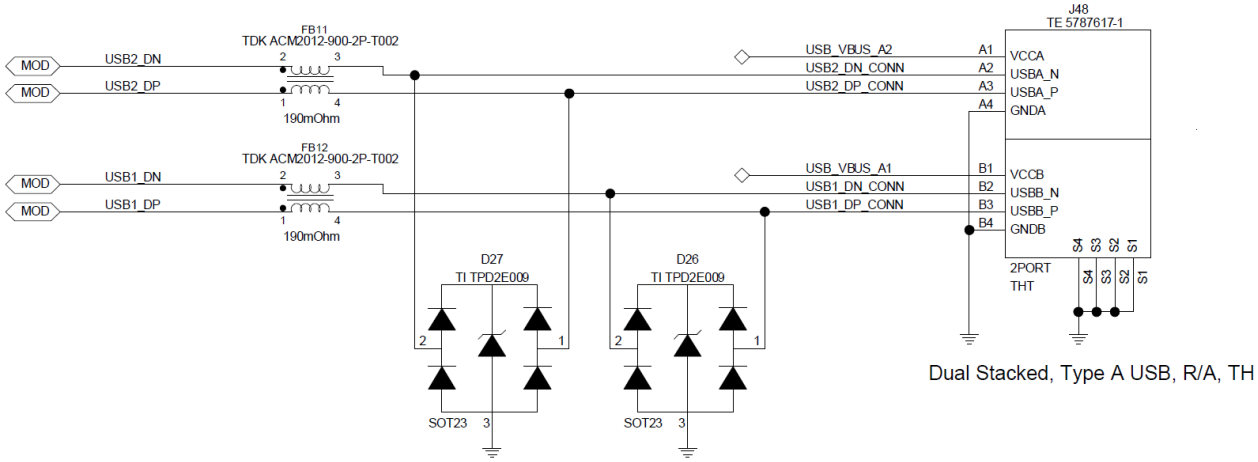


Figure 13 USB 2.0 Host connections

The USB 2.0 OTG connection allows the configuration of the board as Host or Client in function of the wire of connection used for linking both devices (the IGEP™ module and the external device; adapting the SMARC-314 connector lines for an USB type AB). It's defined by the pin P64 (USB0_OTG_ID): when the board detects this pin connected at ground, it will be an A-device; by the other side, if the pin is floating (NC) it will be a B-device. The next figure shows the connections (page 64 of SMARC Design Guide).

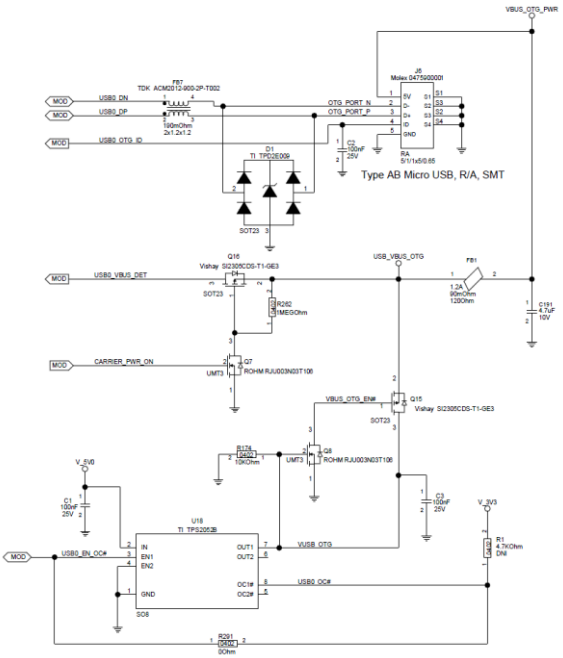


Figure 14 MicroUSB AB 2.0 OTG connections

The USB0_EN_OC# (P62) and USB1_EN_OC# (P67) are, in both cases, optional pins used to detect if there has been an over-consumption (for example a short-circuit). Although in the second example these references are used, it is possible to apply any other of the free GPIO pins if the user wants to implement this feature.

It must be respected a 90Ω (+/-15%) differential impedance in the layout traces when the base board will be designed. At the same time, the traces have to be equal length and symmetric, with regards of shape, length and via count. The differential pairs must be isolated from nearby signals and circuitry to maintain the signal integrity.

To protect the VBUS against overcurrent, the USB power source current have to be less or equal than 500mA, and the user must provide a protection in the base board as it is showed into *Figure 13 USB 2.0 Host connections* and *Figure 14 MicroUSB AB 2.0 OTG connections* examples.

The following table offers the list in the SMARC-314 related pins with both of USB connections.

Pin	Volt Level	Type	Main Function	Comments
USB 2.0 HOST				
P65	USB	IO	USB1+	Analog D+ data pin of the USB1
P66	USB	IO	USB1-	Analog D- data pin of the USB1
P67	3V3	IO OD	USB1_EN_OC#	Active low. Enable Out (active High)-Overcurrent (active Low) pin.
USB 2.0 OTG				
P60	USB	IO	USB0+	Analog D+ data pin of the USB0
P61	USB	IO	USB0-	Analog D- data pin of the USB0
P62	3V3	IO OD	USB0_EN_OC#	Active low. Enable Out (active High)-Overcurrent (active Low) pin.
P63	5V	Input	USB0_VBUS_DET	USB host power detection, when this port is used as a device.
P64	3V3	Input	USB0_OTG_ID	USB OTG ID input, active high

Table 12 USB pins

5.5 I2C: INTER-INTEGRATED CIRCUIT INTERFACE

The IGEP™ SMARC AM335x module can be connected to other peripheral devices by two I2C serial buses. There are eight pins in the SMARC-314 that may be used for this application.

The IGEP™ SMARC AM335x uses a 1V8 voltage levels for I2C buses. In some cases, bidirectional voltage translators should be necessary to adapt voltage levels between ICs. It is important to say that an EEPROM is connected to I2C1. (address 0x50) and TPS65910 is connected to I2C1 (address 0x2D).

In the next example (page 46 of SMARC Design Guide V_IO=1V8) an example of I2C connection is shown.

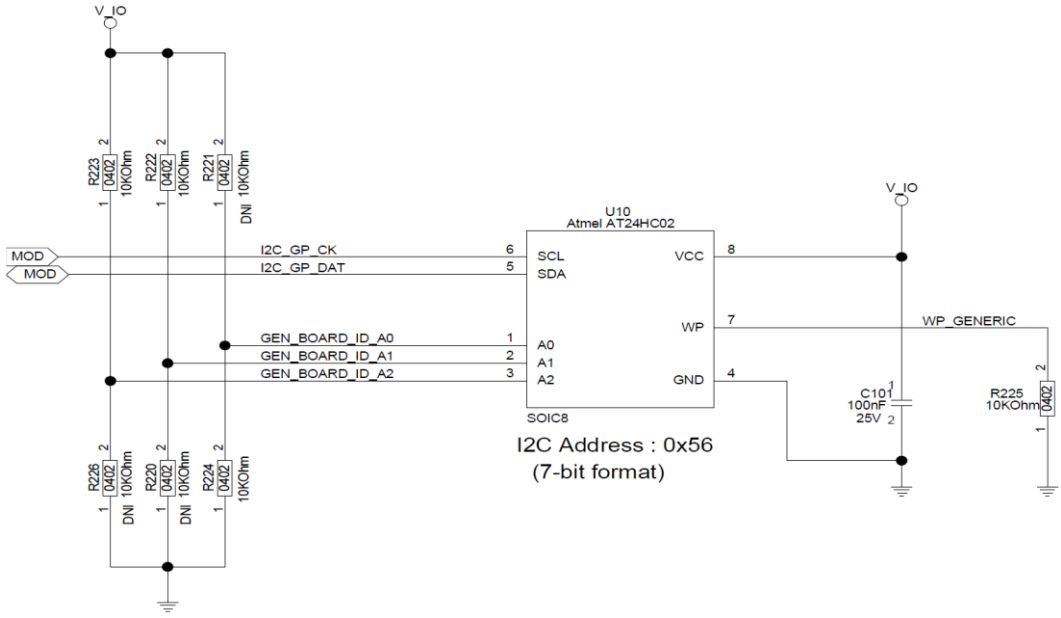


Figure 15 I2C example: EEPROM connection

Pin	Volt Level	Type	Main Function	Comments
I2C1				
P121	1V8	IO OD	I2C_PM_CK	I2C1_SCL: Clock signal. PMIC & EEPROM shared
P122	1V8	IO OD	I2C_PM_DAT	I2C1_SDA: Data signal. PMIC & EEPROM shared
S48	1V8	IO OD	I2C_GP_CK	I2C1_SCL: Clock signal. PMIC & EEPROM shared
S49	1V8	IO OD	I2C_GP_DAT	I2C1_SDA: Data signal. PMIC & EEPROM shared
I2C2				
P105	1V8	IO OD	HDMI_CTRL_CK	I2C2_SCL: Clock signal. Shared with IOExpander (1)
P106	1V8	IO OD	HDMI_CTRL_DAT	I2C2_SDA: Data signal. Shared with IOExpander (1)
S139	1V8	IO OD	I2C_LCD_CK	I2C2_SCL: Clock signal. Shared with IOExpander
S140	1V8	IO OD	I2C_LCD_DAT	I2C2_SDA: Data signal. Shared with IOExpander
Notes				
(1)	I2C Clock and Data lines for HDMI.			

Table 13 I2C pins

5.6 SPI: SERIAL PERIPHERAL INTERFACE

The Serial Peripheral Interface (SPI) is one more of the different possibilities to connect the module to external peripherals. It is a full duplex synchronous bus, supporting a single master and one slave devices each SPI peripheral.

The IGEP™ SMARC AM335x uses a 1V8 voltage levels for SPI buses. In some cases, voltage translators should be necessary to adapt voltage levels between ICs.

In the next figure an example is shown to connect the IGEP™ SMARC AM335x module to an SPI Flash Socket (page 58 of SMARC Design Guide V_IO=1V8).

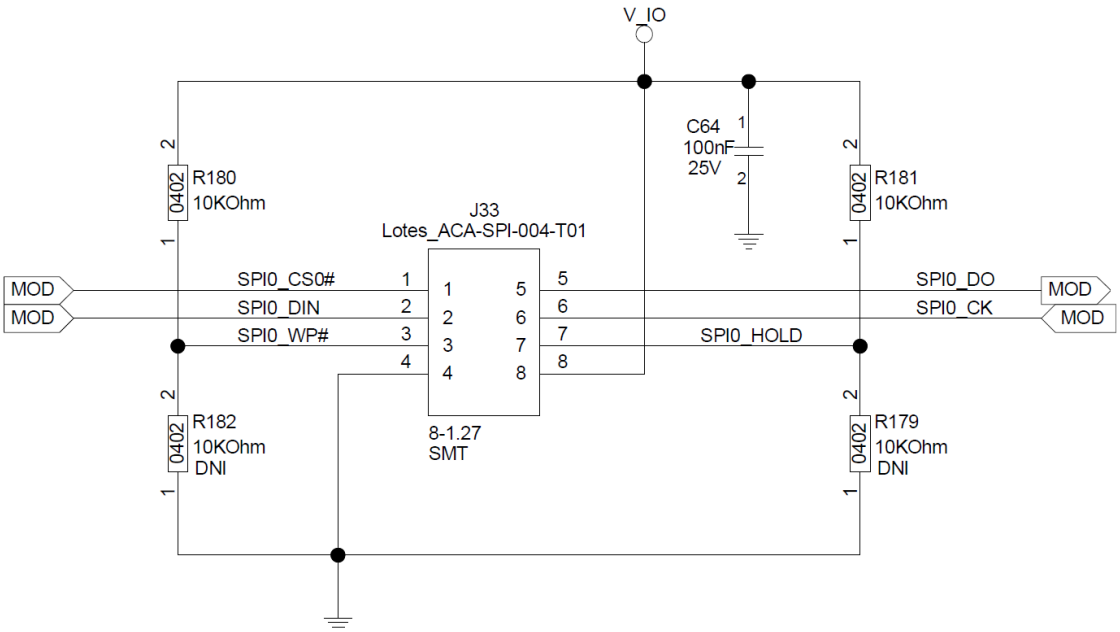


Figure 16 SPI example: SPI Flash Socket

Pin	Volt Level	Type	Main Function	Comments
P31	1V8	Output	SPI0_CS1#	SPI0 Interface: Master Chip Select 1. Active low.
P43	1V8	Output	SPI0_CS0#	SPI0 Interface: Master Chip Select 0. Active low.
P44	1V8	Output	SPI0_CK	SPI0 Interface: Clock.
P45	1V8	Output	SPI0_DIN	SPI0 Interface: Master Data Input. (MISO)
P46	1V8	Output	SPI0_DO	SPI0 Interface: Master Data Output. (MOSI)

Table 14 SPI pins

5.7 WiFi/Bluetooth and SD/MMC CARD (4 bit) INTERFACE

The SMARC AM335x modules contains a certified high-performance WiFi/Bluetooth module with Texas Instruments chipset. Main features are next:

- IEEE 802.11 b/g/n
- Bluetooth 4.2
- Module has an internal antenna.
- Possible to use an external antenna through U.FL jack connector.
- Using external antenna, the cable connected to module must have 50 Ω impedance.

This feature uses control lines from AM335x processor which are shared with other peripheral.

- **UART2 -** This is used to communicate with Bluetooth signals in the WiFi/Bluetooth module (BT_RX, BT_CTS, BT_TX and BT_RTS). If there is not implemented the WiFi/Bluetooth functionality, this can be used as SER2. When WiFi/Bluetooth is installed, these pins in the SMARC-314 interface should float.
- **MCASP0 interface -** This is also used to control the WiFi/Bluetooth module. If there is not present this function, it is available to User the bus I2S0 in the SMARC-314 interface. These pins should be float if WiFi/Bluetooth is implemented.

The IGEP™ SMARC AM335x has two MMC (Multi Media Card) interfaces. The first one (MMC0) is connected to SDIO SMARC pins which allows to install a micro-SD card reader on the Carrier Board, and the second one (MMC1) is used into on-board WiFi module.

The next example shows how to connect a uSD card reader to SDIO pins (page 78 of SMARC Design Guide).

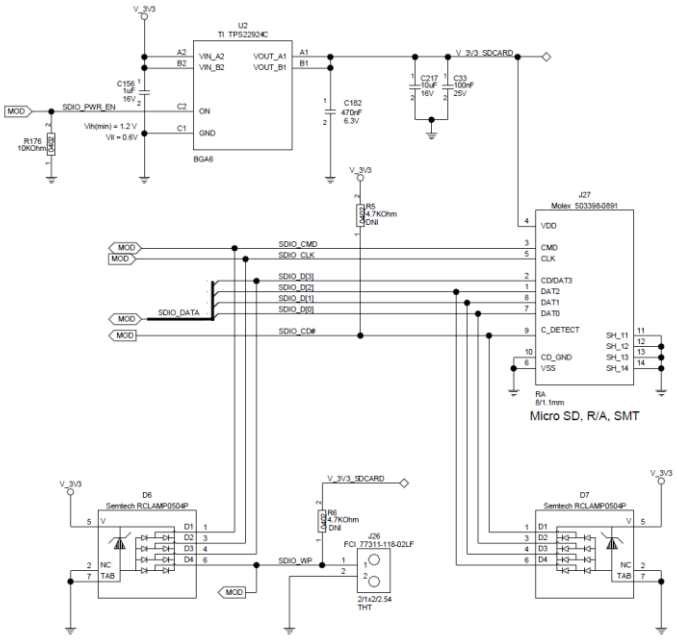


Figure 17 MMC example: uSD card reader

Pin	Volt Level	Type	Main Function	Comments
P33	3V3	Input	SDIO_WP	MMC0 SDIO card 4-bit Interface: Write Protect.
P34	3V3	IO	SDIO_CMD	MMC0 SDIO card 4-bit Interface: Command Line.
P35	3V3	Input	SDIO_CD#	MMC0 SDIO card 4-bit Interface: Card Detect.
P36	3V3	Output	SDIO_CK	MMC0 SDIO card 4-bit Interface: Clock
P37	3V3	Output	SDIO_PWR_EN	MMC0 SDIO card 4-bit Interface: Card Power Enable
P39	3V3	IO	SDIO_D0	MMC0 Data Bus 0. SDIO card 4-bit Interface: data path (D0).
P40	3V3	IO	SDIO_D1	MMC0 Data Bus 1. SDIO card 4-bit Interface: data path (D1).
P41	3V3	IO	SDIO_D2	MMC0 Data Bus 2. SDIO card 4-bit Interface: data path (D2).
P42	3V3	IO	SDIO_D3	MMC0 Data Bus 3. SDIO card 4-bit Interface: data path (D3).

Table 15 SDIO Card Interface pins

5.8 UART: ASYNCHRONOUS SERIAL PORTS

There are three defined UART devices in the module in order to control serial devices or debug via serial. They are available in the SMARC-314 in three blocks of pins.

The IGEP™ SMARC AM335x uses a 1V8 voltage levels for UART buses. In some cases, voltage translators should be necessary to adapt voltage levels between ICs.

The IGEP™ SMARC AM335x uses UART0 as a Kernel Debug Peripheral. This UART is an inexpensive method to detect and repair system issues. It is advisable to use another UART instead of UART0 to preserve this functionality. In the next figure is shown how to connect the UART SMARC pins (page 39 of SMARC Design Guide V_IO=1V8).

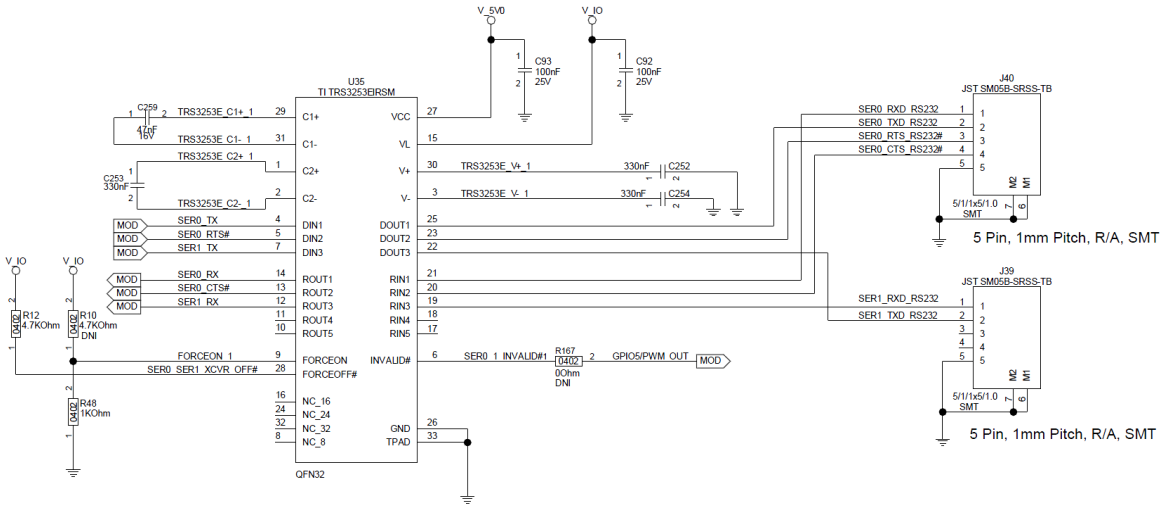
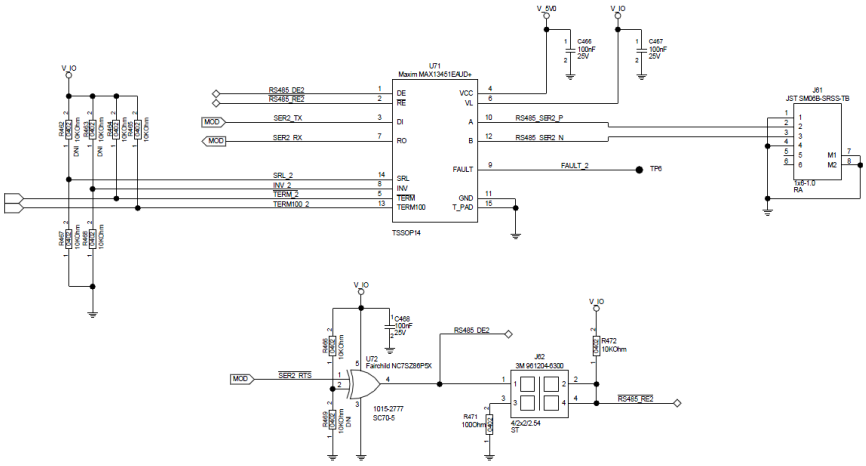


Figure 18 UART SMARC connections

In the next figure is shown another example to use the UART SMARC pins as RS485 bus (page 41 of SMARC Design Guide V_IO=1V8).



Jumper 01-02	Jumper 03-04	State
Open	Open	RS485 reciever disabled
Open	Closed	RS485 reciever always enabled
Closed	Open	RS485 reciever enbled when transmitter disabled
Closed	Closed	Invalid

Figure 19 RS485 example: RS485 circuit

Pin	Volt Level	Type	Main Function	Comments
P129	1V8	Output	SER0_TX	UART3_TX: Asynchronous serial port 1 data output
P130	1V8	Input	SER0_RX	UART3_TX: Asynchronous serial port 1 data input
P134	1V8	Output	SER1_TX	Debug UART0_TX: Asynchronous serial port 1 data output
P135	1V8	Input	SER1_RX	Debug UART0_TX: Asynchronous serial port 1 data input
P136	1V8	Output	SER2_TX	UART2_TX: Asynchronous serial port 1 data output (1)
P137	1V8	Input	SER2_RX	UART2_TX: Asynchronous serial port 1 data output (1)
P138	1V8	Output	SER2_RTS#	UART2_RTS: Request to Send handshake line. Active low. (1)
P139	1V8	Input	SER2_CTS#	UART2_CTS: Clear to Send handshake line. Active low. (1)
P140	1V8	Output	SER3_TX	UART5_TX: Asynchronous serial port 1 data output
P141	1V8	Input	SER3_RX	UART5_TX: Asynchronous serial port 1 data output
Notes				
(1)	This function is only available on modules without Wifi.			

Table 16 Asynchronous Serial Ports pins

5.9 I2S: SERIAL AUDIO PORT

I2S is a synchronous serial bus used for interfacing digital audio devices such as Audio CODECs and DSP chips. Generally, PCM audio data is transmitted over the I2S interface. The I2S bus may have a single bidirectional data line or two separate data lines. The signals constituting the I2S bus are a serial clock/ bit clock (output from the master), a left right clock (output from the master) that indicates the channel being transmitted and a single bidirectional data line or two data lines - one input and one output. A SMARC module can generally be configured as I2S master or slave.

In the next example is connected a Stereo CODEC with Headphone AMP to the Serial Audio Port (page 56 of SMARC Design Guide V_IO=1V8).

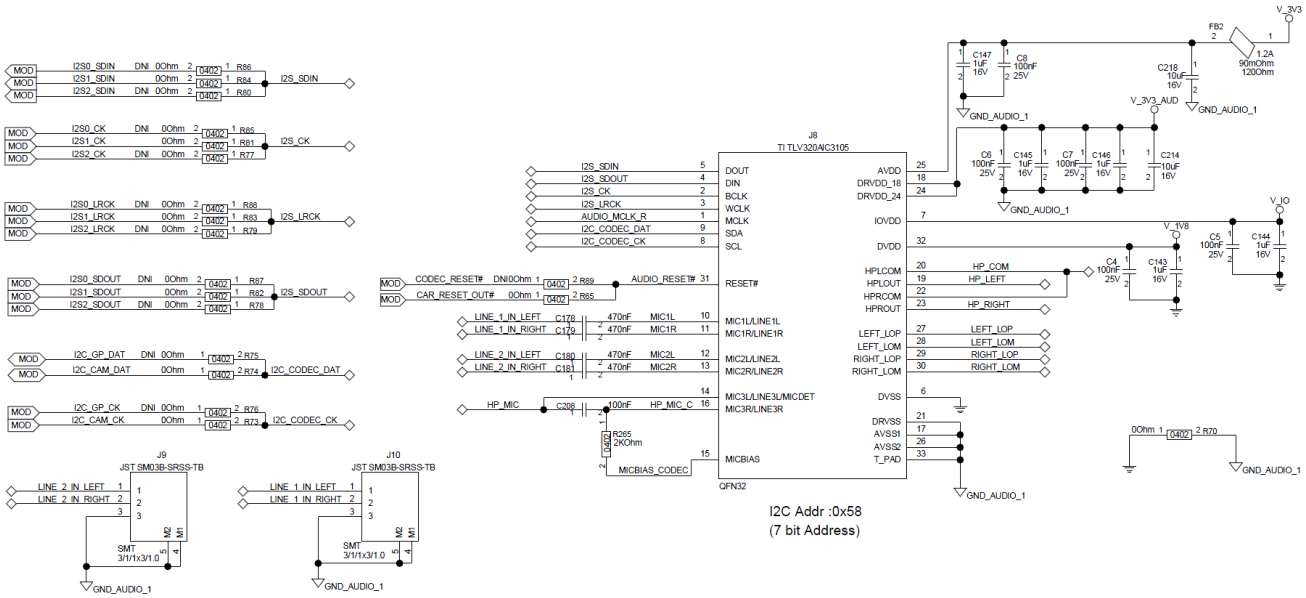


Figure 20 I2S example: Stereo CODEC with Headphone AMP

Pin	Volt Level	Type	Main Function	Comments
S38	1V8	Output	AUDIO_MCK	I2S: Master clock output to Audio codecs. 12MHz Clock.
S39	1V8	IO	I2S0_LRCK	MCASP0_FSX: Left & Right Audio Frame synchronization clock.
S40	1V8	Output	I2S0_SDOUT	MCASP0_AXR0: Digital Audio output signal.
S41	1V8	Input	I2S0_SDIN	MCASP0_AXR1: Digital Audio input signal.
S42	1V8	IO	I2S0_CK	MCASP0_ACLKX: Digital Audio Clock signal.

Table 17 I2S pins

5.10 CAN BUS: CONTROLLER AREA NETWORK

The module can be integrated in a global system using the serial standard CAN Bus. The CAN Bus is a standard designed to allow microcontrollers and devices to communicate with each other without a host computer. It is a differential half duplex data bus, using shielded or unshielded twisted differential pair wiring, with an impedance termination of 120Ω at the endpoints of the bus. Nodes on the bus are arranged in daisy-chain fashion.

There are two available CAN ports.

A CAN Transceiver is needed on the baseboard to connect the system to the CAN Bus. In the next example (page 61 of SMARC Design Guide V_IO=1V8), are showing this application using the NCV7341 chip (it is a high-speed CAN Transceiver).

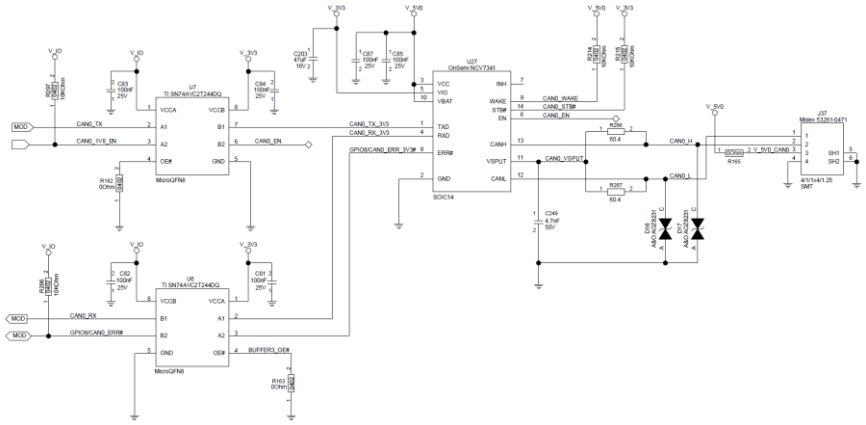


Figure 21 CAN Bus circuit example

Pin	Volt Level	Type	Main Function	Comments
P143	1V8	Output	CAN0_TX	CAN0 Transmission Line (TX)
P144	1V8	Input	CAN0_RX	CAN0 Reception Line (RX)
P145	1V8	Output	CAN1_TX	CAN1 Transmission Line (TX)
P146	1V8	Input	CAN1_RX	CAN1 Reception Line (RX)

Table 18 CAN Bus pins

5.11 GPIO: GENERAL PURPOSE INPUT OUTPUT

GPIOs are input/output (IO) general purpose pins used to control LEDs, relays, switch, etc. In the next figure is shown a basic circuit with an input pushbutton and two outputs to manage LED signals.

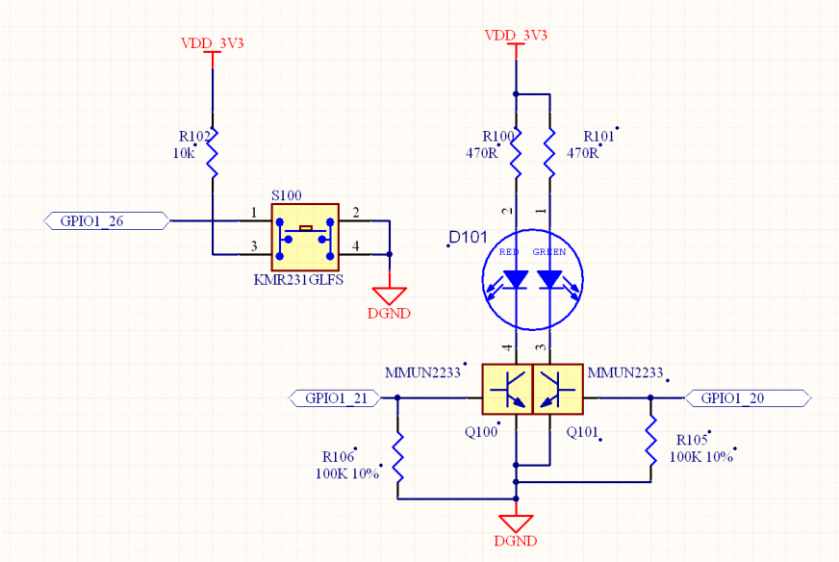


Figure 22 GPIOs example: control circuit to manage LEDs

Pin	Volt Level	Type	Main Function	Comments
P108	1V8	IO	GPIO0	AM335x General purpose input/output (GPIO0_23)
P109	1V8	IO	GPIO1	GPIO FROM IOMUX P13 (I2C2)
P110	1V8	IO	GPIO2	GPIO FROM IOMUX P14 (I2C2)
P111	1V8	IO	GPIO3	GPIO FROM IOMUX P15 (I2C2)
P112	1V8	IO	GPIO4	GPIO FROM IOMUX P16 (I2C2)
P113	1V8	IO	GPIO5 - PWM	AM335x EHRPWM2A or GPIO0_22 (1)
P114	1V8	IO	GPIO6	GPIO FROM IOMUX P20 (I2C2)
P115	1V8	IO	GPIO7	GPIO FROM IOMUX P21 (I2C2)
P116	1V8	IO	GPIO8	GPIO FROM IOMUX P22 (I2C2)
P117	1V8	IO	GPIO9	GPIO FROM IOMUX P23 (I2C2)
P118	1V8	IO	GPIO10	GPIO FROM IOMUX P24 (I2C2)
P119	1V8	IO	GPIO11	GPIO FROM IOMUX P25 (I2C2)
S35	1V8	IO	GPIO	GPIO1_30
S36	1V8	IO	GPIO	GPIO1_31
Notes				
(1)	P113 could be use as PWM signal or as digital GPIO, depends on how you configure the AM335x			

Table 19 GPIO pins

5.12 ANALOG INPUTS

The SMARC AM335x has available eight analog inputs.

Please, be careful because these inputs are unprotected and maximum voltage is 1V8.

Pin	Volt Level	Type	Main Function	Comments
P3	1V8	Input	AIN0	Analog Input 0 (1)
P4	1V8	Input	AIN1	Analog Input 1 (1)
P7	1V8	Input	AIN2	Analog Input 2 (1)
P8	1V8	Input	AIN3	Analog Input 3 (1)
P10	1V8	Input	AIN4	Analog Input 4 (1)
P11	1V8	Input	AIN5	Analog Input 5 (1)
P13	1V8	Input	AIN6	Analog Input 6 (1)
P14	1V8	Input	AIN7	Analog Input 7 (1)
Notes				
(1)	Unprotected. Maximum 1,8 V			

Table 20 Analog Inputs pins

5.13 DVI

The SMARC AM335x has available a DVI display interface and the DVI data pairs may be routed directly from the SMARC-314 interface pins to a suitable Carrier HDMI connector.

Since DVI is a hot-plug capable interface, it is important for the Carrier to implement ESD protection on all of the DVI lines. The ESD protection on the data lines must be low capacitance so as not to degrade high speed signalling. The data lines must route through the ESD protection device pins in a no-stub fashion. The ESD protection should be located close to the HDMI connector.

Information to DVI transmitter is made through the parallel output from AM335x processor, so in case to use the DVI output there is information in the LCD pins of SMARC-314 interface. **When it is used the DVI output, should be not used an unconnected to the Carrier Board the LCD outputs.**

The next figure shows how to connect SMARC DVI pins to HDMI connector (page 35 of SMARC Design Guide V_IO=1V8).

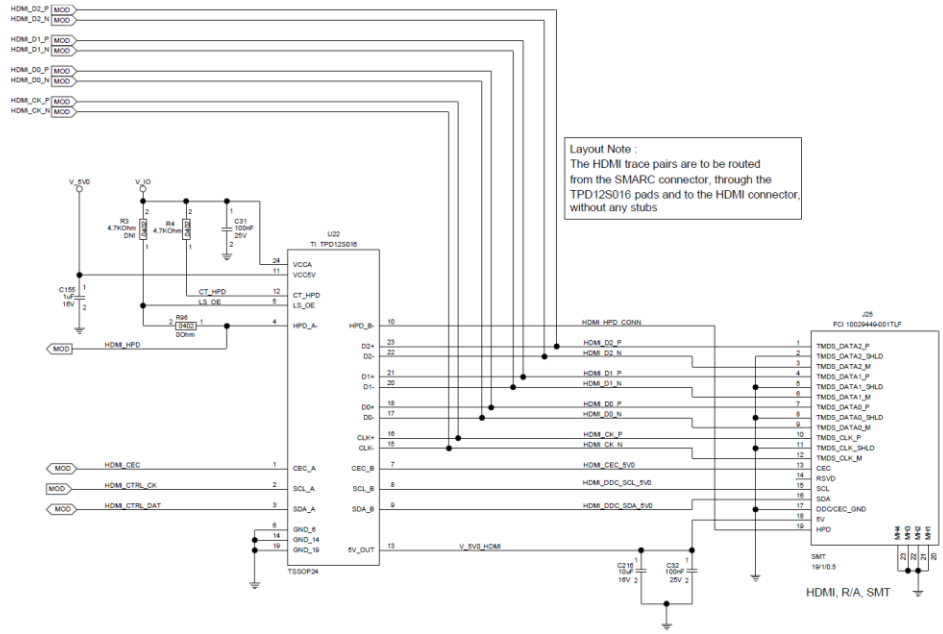


Figure 23 HDMI connection example

Pin	Volt Level	Type	Main Function	Comments
P92	TMDS	Output	DVI_D2+	DVI data differential pair D2 +
P93	TMDS	Output	DVI _D2-	DVI data differential pair D2 -
P95	TMDS	Output	DVI_D1+	DVI data differential pair D1 +
P96	TMDS	Output	DVI_D1-	DVI data differential pair D1 -
P98	TMDS	Output	DVI_D0+	DVI data differential pair D0 +
P99	TMDS	Output	DVI_D0-	DVI data differential pair D0 -
P101	TMDS	Output	DVI_CK+	DVI differential clock output pair +
P102	TMDS	Output	DVI_CK-	DVI differential clock output pair -
P105	1V8	Output OD	HDMI_CTRL_CK	I2C Clock line for HDMI. Shared with IOExpander.
P106	1V8	IO OD	HDMI_CTRL_DAT	I2C Data line for HDMI. Shared with IOExpander

Table 21 DVI pins

5.14 LCD

The SMARC AM335x has also available a parallel output display (LCD outputs in SMARC-314 interface). These are connected directly to AM335x processor LCD pins, and they are the same pins used to send information to DVI transmitter.

When it is used the DVI output, should be not used an unconnected to the Carrier Board the LCD outputs.

Pin	Volt Level	Type	Main Function	Comments
S96	1V8	Output	LCD_D0	LCD_DATA0 (Blue0)
S97	1V8	Output	LCD_D1	LCD_DATA1 (Blue1)
S98	1V8	Output	LCD_D2	LCD_DATA2 (Blue2)
S99	1V8	Output	LCD_D3	LCD_DATA3 (Blue3)
S100	1V8	Output	LCD_D4	LCD_DATA4 (Blue4)
S104	1V8	Output	LCD_D5	LCD_DATA5 (Green0)
S105	1V8	Output	LCD_D6	LCD_DATA6 (Green1)
S106	1V8	Output	LCD_D7	LCD_DATA7 (Green2)
S107	1V8	Output	LCD_D8	LCD_DATA8 (Green3)
S108	1V8	Output	LCD_D9	LCD_DATA9 (Green4)
S109	1V8	Output	LCD_D10	LCD_DATA10 (Green5)
S114	1V8	Output	LCD_D11	LCD_DATA11 (Red0)
S115	1V8	Output	LCD_D12	LCD_DATA12 (Red1)
S116	1V8	Output	LCD_D13	LCD_DATA13 (Red2)
S117	1V8	Output	LCD_D14	LCD_DATA14 (Red3)
S118	1V8	Output	LCD_D15	LCD_DATA15 (Red4)
S120	1V8	Output	LCD_DE	LCD_AC_BIAS_ENABLE
S121	1V8	Output	LCD_VS	LCD_VSYNC
S122	1V8	Output	LCD_HS	LCD_HSYNC
S123	1V8	Output	LCD_PCK	LCD_CLK
S127	1V8	Output	LCD_BKLT_EN	GPIO FROM IOMUX P27 (I2C2) LCD Panel Backlite Enable
S133	1V8	Output	LCD_VDD_EN	GPIO FROM IOMUX P26 (I2C2) LCD Panel Power Enable
S141	1V8	Output	LCD_ BKLT_PWM	LCD Panel Backlite PWM signal EHRPWM2A or GPIO0_22

Table 22 LCD pins

5.15 RTC BATTERY

The RTC Battery pin (S147) allows the connection of a battery. With this, in case of a general power fall, RTC circuit will be powered. The user has to be careful with the selection of battery capacity: depending on the current consumption, the activity duration will be drastically reduced.

Next figure shows RTC Battery examples (page 30 of SMARC Design Guide).

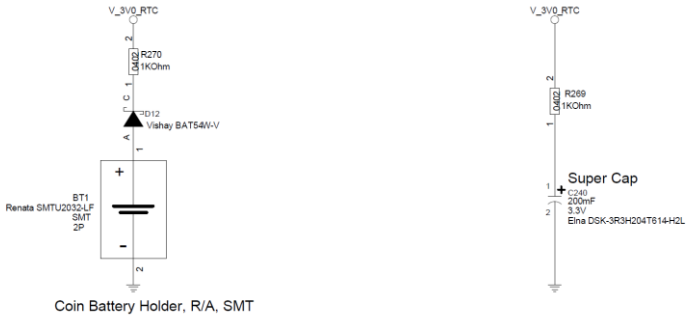


Figure 24 RTC Battery

The Carrier Board must be implemented the needed circuits to protect against charging by reverse currents.

Pin	Volt Level	Type	Main Function	Comments
S147	3V0	Power	VDD_RTC	Low current RTC circuit backup power – 3.0V nominal. May be sourced from a Carrier based lithium cell or super cap.

Table 23 RTC Battery pin

5.16 ENVIRONMENTAL SPECIFICATION

General Specification	Operating	Non-operating
Industrial grade (E2)	-40ºC to +80ºC	-40ºC to +80ºC

Table 24 Temperature range

Standard modules are available for Industrial grade temperature range. The operating temperature is the maximum measurable temperature on any spot on the module's surface.

- **Humidity**

93% relative Humidity at 40ºC, non-condensing (according to IEC 60068-2-78).

5.17 STANDARDS AND CERTIFICATIONS

- **RoHS**

lead-free RoHS 2002/95/EC

The SMARC AM335x is compliant to the directive 2002/95/EC on the restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment.

- **CE Marking**

The SMARC AM335x is CE marked according to Low Voltage Directive 2006/95/EC – Test standard EN60950.

- **WEEE Directive**

WEEE Directive 2002/96/EC is not applicable for Computer-on-Modules.

- **Conformal Coating**

Conformal Coating is available for Computer-on-Modules and for validated SMARC modules. Please, contact your local sales or support for further details.

- **EMC**

The SMARC AM335x is designed and tested following EN55022 standard ("INFORMATION TECHNOLOGY EQUIPMENT. RADIO DISTURBANCE CHARACTERISTICS. LIMITS AND METHODS OF MEASUREMENT").

- **SMARC Form Factor standard**

The SMARC ("Smart Mobility Architecture") is a versatile small form factor computer Module definition targeting application that require low power, low costs and high performance.

5.18 MTBF

The SMARC AM335x has been designed with a predicted MTBF (Mean Time Before Failure) of >131400 hours (>15 years).

All hardware components are selected with long time industrial reliability parameters. The MTBF prediction of hardware components and temperature stress could be estimated, but the newest devices are very software dependent. So, final application has an important effect on MTBF.

5.19 MECHANICAL SPECIFICATION

- **Module Dimension**

82,00 mm x 50,00 mm x 4,30 mm (high without JTAG connector)

- **Mechanical Drawing**

The next figures show the SMARC AM335x modules mechanical dimensions:

  - All dimensions are in millimeters.
  - 8-layer Printed Circuit Board size is 82,00 mm x 50,00 mm x 1,15 mm.
  - Mounting holes are provided, one on each corner.

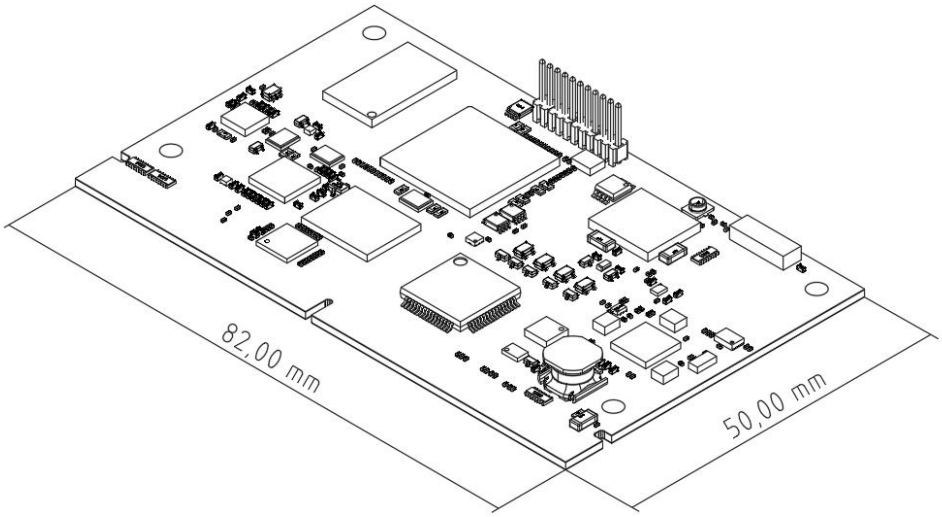


Figure 25 SMARC AM335x Outline dimensions

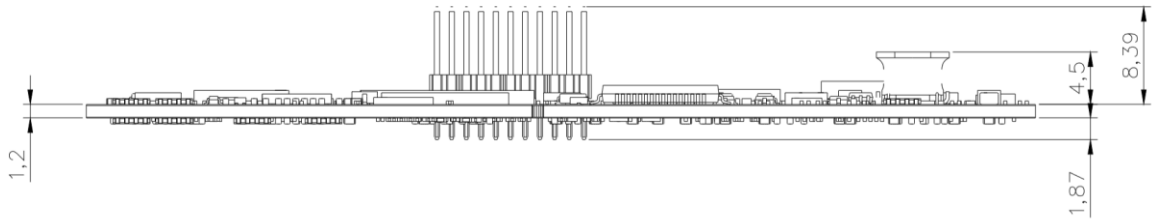


Figure 26 SMARC AM335x Lateral view widths dimensions

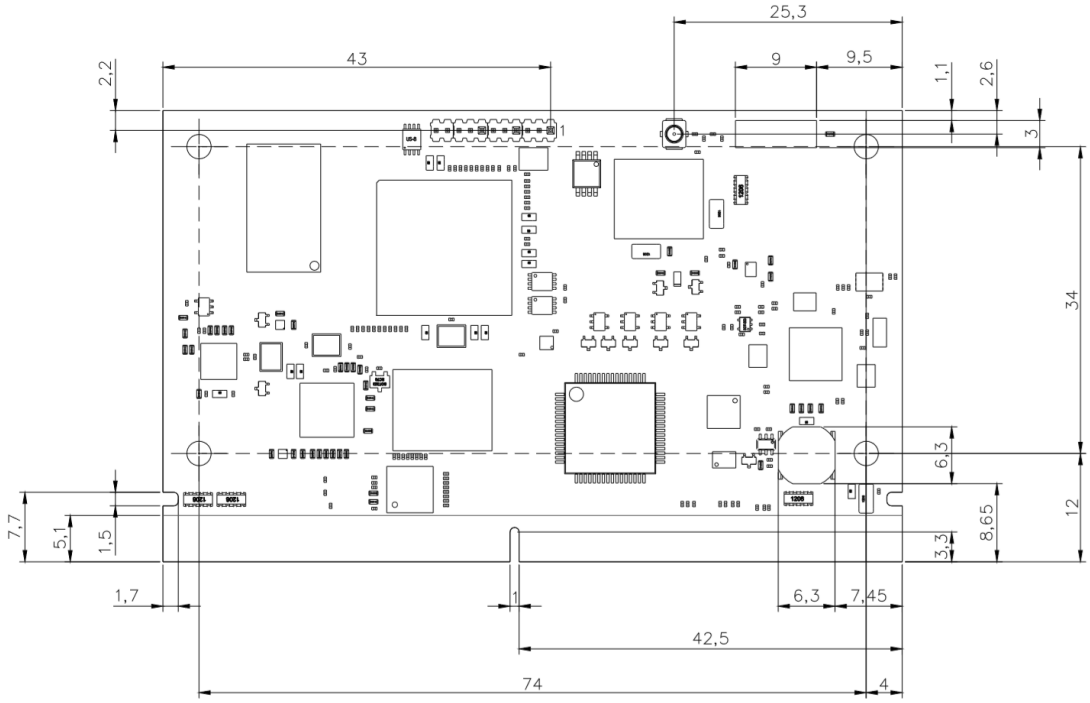


Figure 27 SMARC AM335x Side view detailed mechanical dimension

6 ON-BOARD INTERFACES

6.1 SUMMARY

Device	Connector	Reference	Description
LED	-	D100	GPIO controlled
JTAG	11-pin 1,25 mm pitch interface	JTAG	-

Table 25 Interface summary

6.2 LEDs

The SMARC AM335x module provides a bicolor LED indicator on the board. They can be controlled by the user through GPIOs.

Signal Name	LED Color	Description
LED_R	D100 Red	Controlled by GPIO0_26 of AM335x
LED_G	D100 Green	Controlled by GPIO0_27 of AM335x

Table 26 LEDs

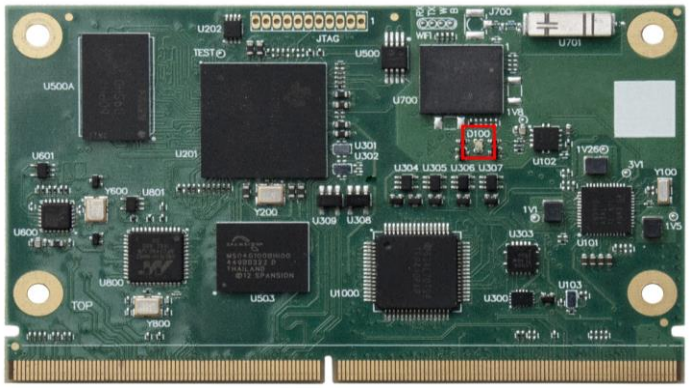


Figure 28 LEDs position in the PCB

6.3 JTAG

The SMARC AM335x provides a footprint JTAG interface to help in the developing of user's code.

The JTAG port is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG). Support IEEE P1149.6 extensions to the JTAG standard are for AC testing of selected IO signals.

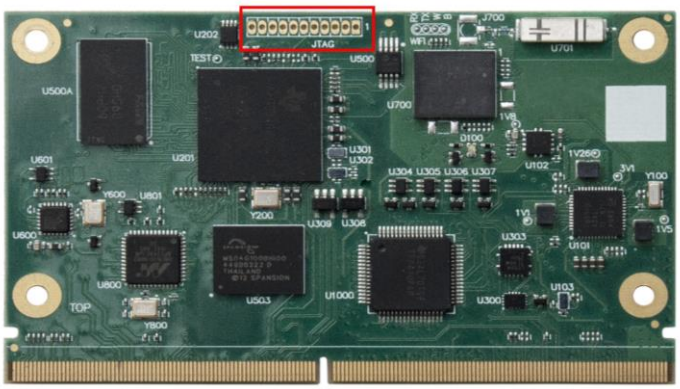


Figure 29 JTAG position in the PCB

Next figure shows the pinout schematic and the corresponding metal contacts.

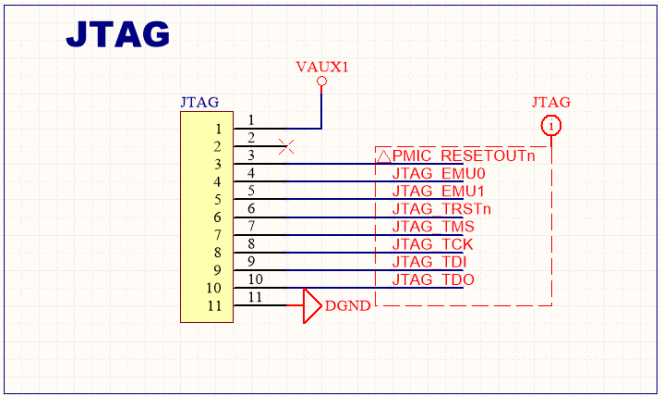


Figure 30 JTAG connector schematic

Note that even pins are left unconnected, but the footprint makes possible to use a 11 pin 1.27 mm pitch connector. Next table details the signals on each pin.

Signal Name	JTAG pin	Description
VAUX1	1	1,8 V power supply.
NC	2	Not Connected.
PMIC_RESETOUTn	3	System Reset Signal
JTAG_EMU0	4	EMU0 / GPIO3_7
JTAG_EMU1	5	EMU1 / GPIO3_8
JTAG_NTRST	6	JTAG Test Reset Input Signal.
JTAG_TMS	7	JTAG Test Mode Select Input Signal.
JTAG_TCK	8	JTAG Test Clock Input Signal.
JTAG_TDI	9	JTAG Test Data Input Signal.
JTAG_TDO	10	JTAG Test Data Output Signal.
GND	11	Ground.

Table 27 JTAG pinout

7 ELECTRICAL CHARACTERISTICS

Electrical parameter	Min	Typ	Max	Unit
5 V INPUT POWER SUPPLY				
SMARC AM335x Input Power Supply Voltage	4.5	-	5.25	V
SMARC AM335x Input Power Supply Current (1)	-	0.32	2	A
Input/Output pins (2)				
Output High-Level DC Voltage	1.6	-	1.8	V
Input High-Level DC Voltage	1.26	-	1.8	V
Output Low-Level DC Voltage	-	-	0.2	V
Input Low-Level DC Voltage	0	-	0.54	V
RTC_BATTERY type pins				
Input DC Voltage	2.5	3	3.25	V

Table 28 SMARC AM335x Electrical Characteristics

(1) Current measured with default delivered software. Be aware that different software configurations could drastically modify current consumption.

(2) The electrical specification depends on the configured mode. For accurate information of each pin, revise AM335x Applications Processor official document from Texas Instruments official site http://www.ti.com.

SMARC AM335x MODULES CAN BE DAMAGED IF ANY OF THESE ELECTRICAL LIMITS ARE EXCEEDED AND/OR ELECTROSTATIC DISCHARGE PRECAUTIONS ARE NOT FOLLOWED.

WARRANTY LOST IF IMPROPER USE OF THE MODULE IS FOUND.

8 EXPANSION BOARD

All the products in the SMARC AM335x series can be supplemented with next expansion board.

Part Number	IGEP™ Device	Description
BASE0040-DFEV-UGAC	BASE SMARC EXPANSION	Designed for fast prototyping of user's projects

Table 29 BASE SMARC EXPANSION Ordering Information

The BASE SMARC EXPANSION is a fully equipped baseboard that access to almost all SMARC functionalities. It has been designed to be used as the fastest way to develop and check the user's final application before building a prototype, saving costs and reducing time to market.

This model can be used with all the ISEE ASSEMBLY TECHNOLOGY's SMARC series modules. Thanks to this design, the user only needs to purchase one Expansion board to check all SMARC modules manufactured by ISEE ASSEMBLY TECHNOLOGY.

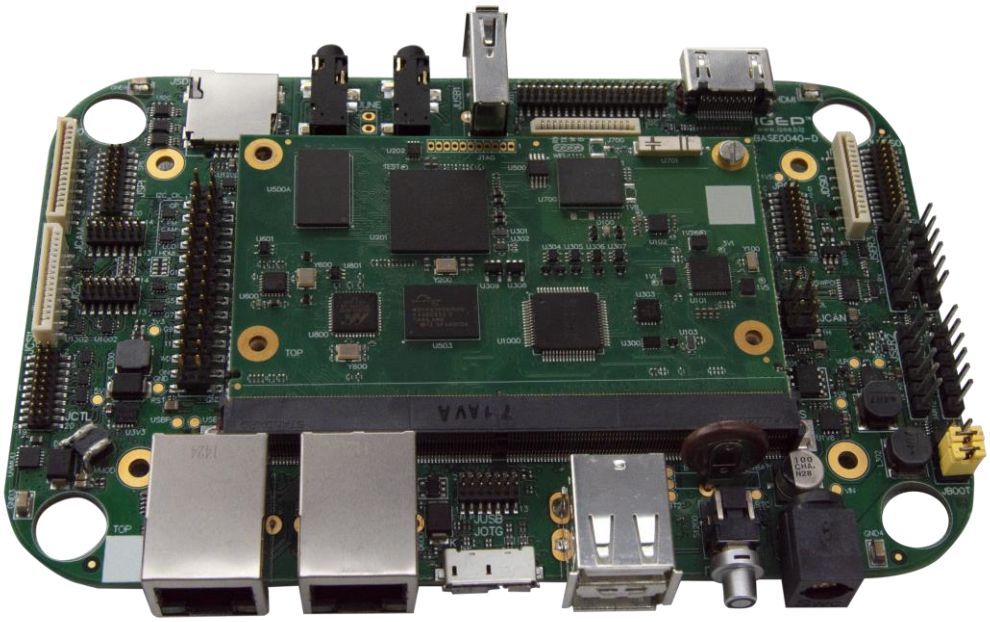


Figure 31 BASE0040 SMARC EXPANSION

The following table contains all the features and capabilities of the BASE SMARC EXPANSION.

Connectors	Features	Dimensions	Case Dimensions
1 x SMARC connector 1 x Power Supply (+5 V) connector 2 x 10/100/1000 Mbps Base RJ45 1 x HDMI Type A receptacle 1 x LCD 24-bit connector 1 x Touchscreen connector 1 x XLCD expansion 40-pin header 1 x LVDS expansion 24-pin header 2 x CSI connector, 2-lanes 1 x Parallel Camera expansion 14-pin header 1 x Stereo Line Input Mic/Line 1 x Stereo Line Output Headphone 1 x I2S 14-pin header 3 x USB 2.0 Type A receptacle 1 x USB 3.0 Type AB receptacle 1 x USB2 expansion 14-pìn header 1 x Modem USB & PCIe interface 1 x mSATA & PCIe interface 1 x PCI expansion 20-pin header 1 x Micro-SD connector 1 x SIM-card connector 2 x DSI connector 2 x CAN on a 6-pin header 1 x SPI 20-pin header 1 x I/O expansion 28-pin header 4 x Serial UART 3V3 expansion 6-pin header	1 x Button-LED (2 LEDs: red, blue) 3 x Boot jumpers 1 x Control 20-pin header	142,00 mm x 90,00 mm (without case)	150,00 mm x 100,00 mm x 30,00 mm

Table 30 BASE0040 SMARC EXPANSION Features Rev. D

9 Document and Standards References

- **CAN** (“Controller Area Network”) Bus Standards
  ISO 11898-1:2015 Road vehicles - Controller area network (CAN) - Part 1: Data link layer and physical signaling, (https://www.iso.org)
  ISO 11992-1:2019 Road vehicles - Interchange of digital information on electrical connections between towing and towed vehicles - Part 1: Physical and data-link layers (https://www.iso.org)
  SAE J2411: Feb 14, 2000, Single Wire CAN Network for Vehicle Applications (https://www.sae.org)
- **MIPI CSI-2** (Camera Serial Interface version 2) The MIPI CSI-2 standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- **MIPI CSI-3** (Camera Serial Interface version 3) The MIPI CSI-3 standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- **COM Express** – the formal title for the COM Express specification is “PICMG® COM.0 COM Express Module Base Specification”, Revision 3.0, March 31, 2017. This standard is owned and maintained by the PICMG (“PCI Industrial Computer Manufacturer’s Group”) (www.picmg.org)
- **DisplayPort and Embedded DisplayPort -** These standards are owned and maintained by VESA (“Video Electronics Standards Association”) (www.vesa.org)
- **MIPI DSI** (Display Serial Interface) The DSI standard is owned and maintained by the MIPI Alliance (“Mobile Industry Processor Alliance”) (www.mipi.org)
- **eMMC** (“Embedded Multi-Media Card”) The eMMC electrical standard is defined by JEDEC JESD84-B51A and the mechanical standard by JESD84-C44 (www.jedec.org)
- **eSPI** (“Enhanced Serial Peripheral Interface”) The eSPI Interface Base Specification is defined by Intel (https://www.intel.com)
- **Fieldbus** - this term refers to a number of network protocols used for real – time industrial control. Refer to the following web sites: https://www.profibus.com/download/ and www.can-cia.org
- **GBE MDI** (“Gigabit Ethernet Medium Dependent Interface”) This is defined by IEEE 802.3. The 1000Base-T operation over copper twisted pair cabling is defined by IEEE 802.3ab (www.ieee.org)
- **HDA (HD Audio),** High Definition Audio Specification, Intel, Revision 1.0a, June 17, 2010 (http://www.intel.com)
- **HDMI Specification,** Version 2.1, November 28, 2017 (www.hdmi.org)
- **I2C Specification,** Version 6.0, April 4th 2014, Philips Semiconductor (now NXP) (www.nxp.com)
- **I2S Bus Specification**, Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com)
- **IEEE1588 - 2008**. IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems (http://standards.ieee.org)
- **JTAG** (“Joint Test Action Group”) This is defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (https://ieeexplore.ieee.org)
- **MXM3** Graphics Module Mobile PCI Express Module Electromechanical Specification, Version 3.1, NVidia Corporation
- **PICMG® EEEP** Embedded EEPROM Specification, Rev. 1.0, August 2010 (www.picmg.org)
- **PCI Express** Specifications (www.pci-sig.org)
- **Serial ATA** Revision 3.1, July 18, 2011, Gold Revision, © Serial ATA International Organization (www.sata-io.org) SMARC 2.1.1 Specification © 2020 SGET e.V. Page 9 of 109
- **SD Specifications** Part 1 Physical Layer Simplified Specification, Version 6.00, Aug 29, 2018, SD Group and SD Card Association (“Secure Digital”) (www.sdcard.org)
- **SM Bus** – “System Management Bus” Specification Version 3.1, March 19, 2018, System Management Interface Forum, Inc. (http://www.smbus.org)

- **SPI Bus** – “Serial Peripheral Interface” – de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus)
- **USB** Specifications (http://www.usb.org)